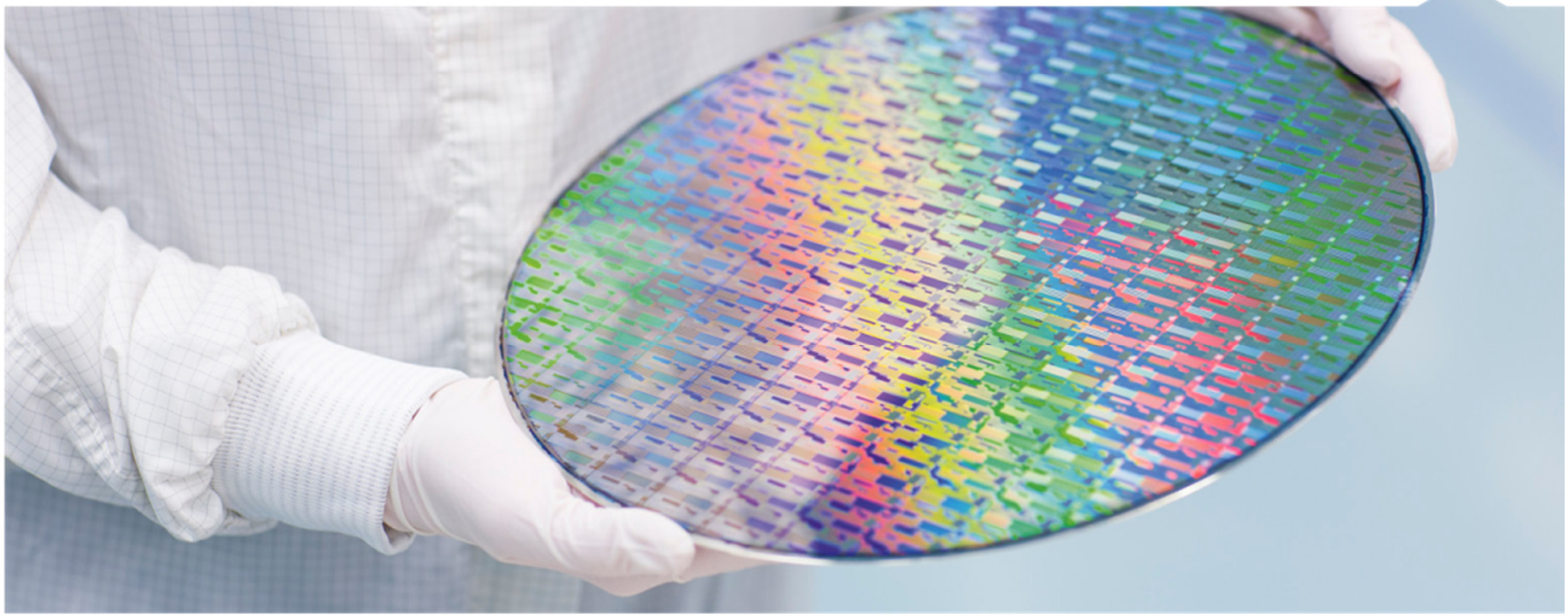
DRIVE INNOVATION · DELIVER EXCELLENCE >

ASM



ENABLING ADVANCED CHIP MANUFACTURING WITH NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 9, 2014

SAFE HARBOR STATEMENTS

Safe Harbor Statement under the U.S. Private Securities Litigation Reform Act of 1995: All matters discussed in this business and strategy update, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholder and other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's filings from time to time with the U.S. Securities and Exchange Commission, including, but not limited to, the Company's reports on Form 20-F and Form 6-K. The company assumes no obligation to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **New Materials: Moore's law enablers**
- **ALD as enabler of new materials**
  - What is Atomic Layer Deposition (ALD)?
  - Key strengths of ALD
- **ASM and ALD**
- **ASM Products and selected applications**
- **Summary and Conclusions**

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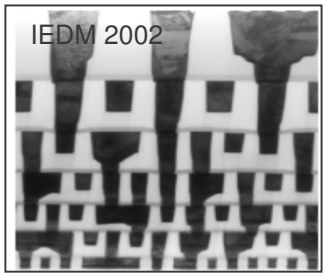
SCALING IS INCREASINGLY ENABLED BY NEW MATERIALS AND 3D TECHNOLOGIES

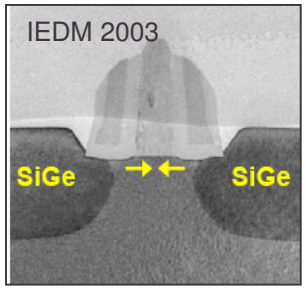
1990 1995 2000 2005 2010 2015 2020 2025

Scaling enabled by Litho

Double / Quad Patterning



Scaling enabled by Materials

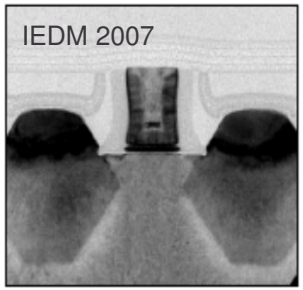


Low-k

Strained Si

High-k

High-mobility channel materials



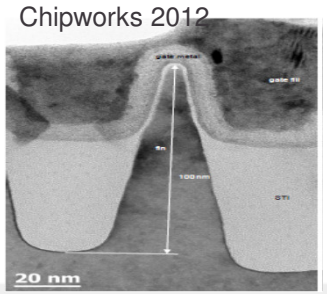
Scaling enabled by 3D

FinFET

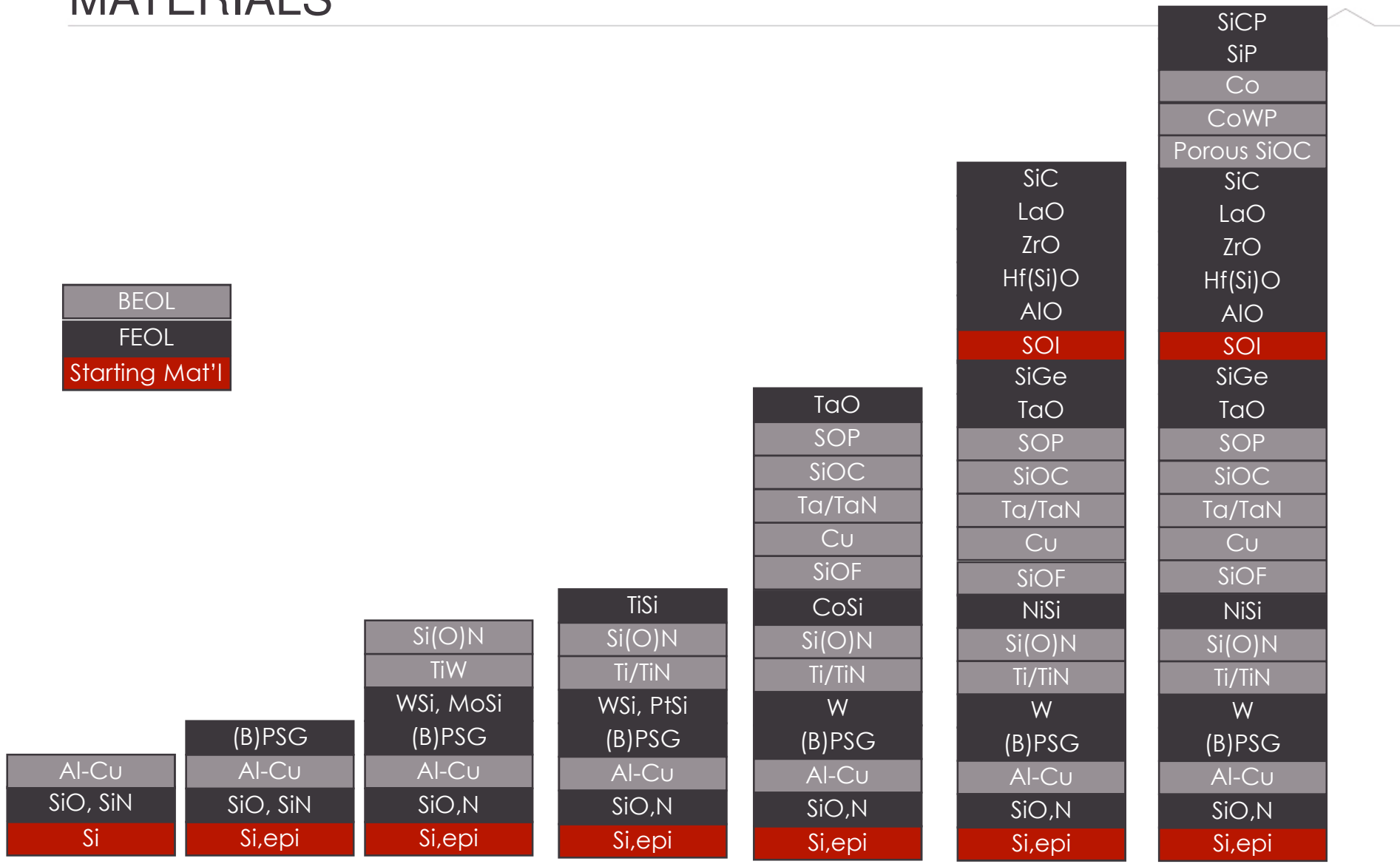
3D SIC

3D Memory

GAA

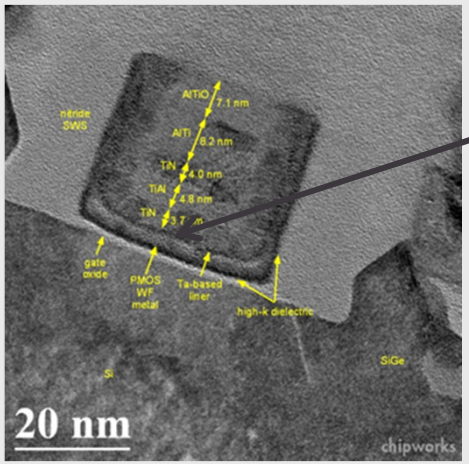


INCREASING INTRODUCTION RATE OF NEW MATERIALS



NEW MATERIALS AND PROCESSES: MOORE'S LAW ENABLERS

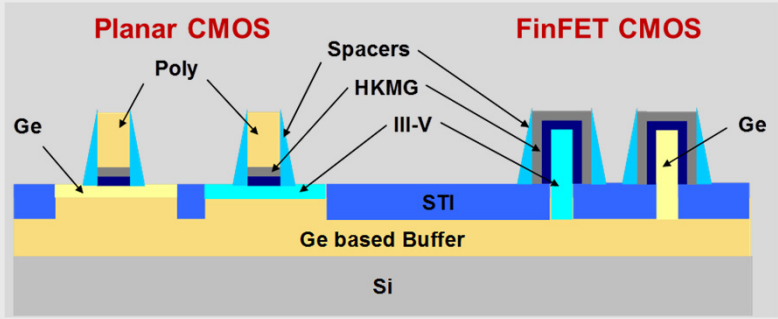
Higher Capacitance, Lower Leakage



High-k and Metal Gates

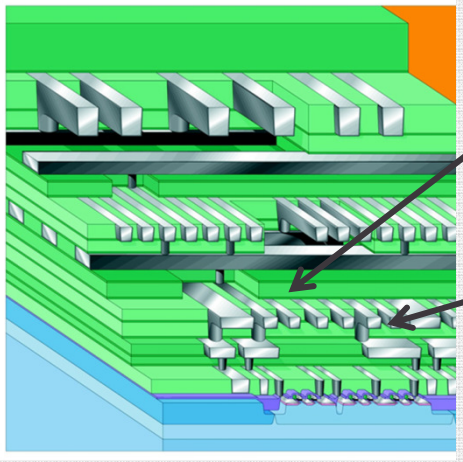
DRAM, RF, decoupling capacitors

Higher Mobility, Lower Resistance



Strain and new Channel Materials
New metal contacts

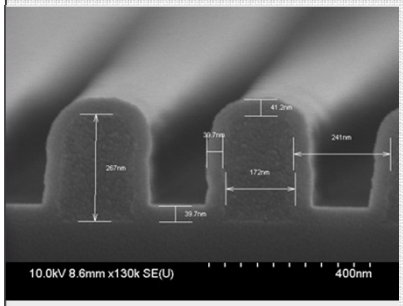
Less Cross Talk, Faster Interconnect



(Porous) Low-k Materials

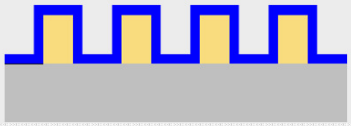
Improved Metals

Smaller Feature Sizes

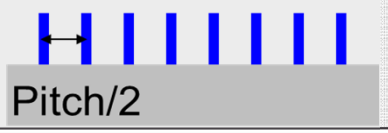


Sub-Rayleigh limit patterning using SDDP

Conformal SiO_2

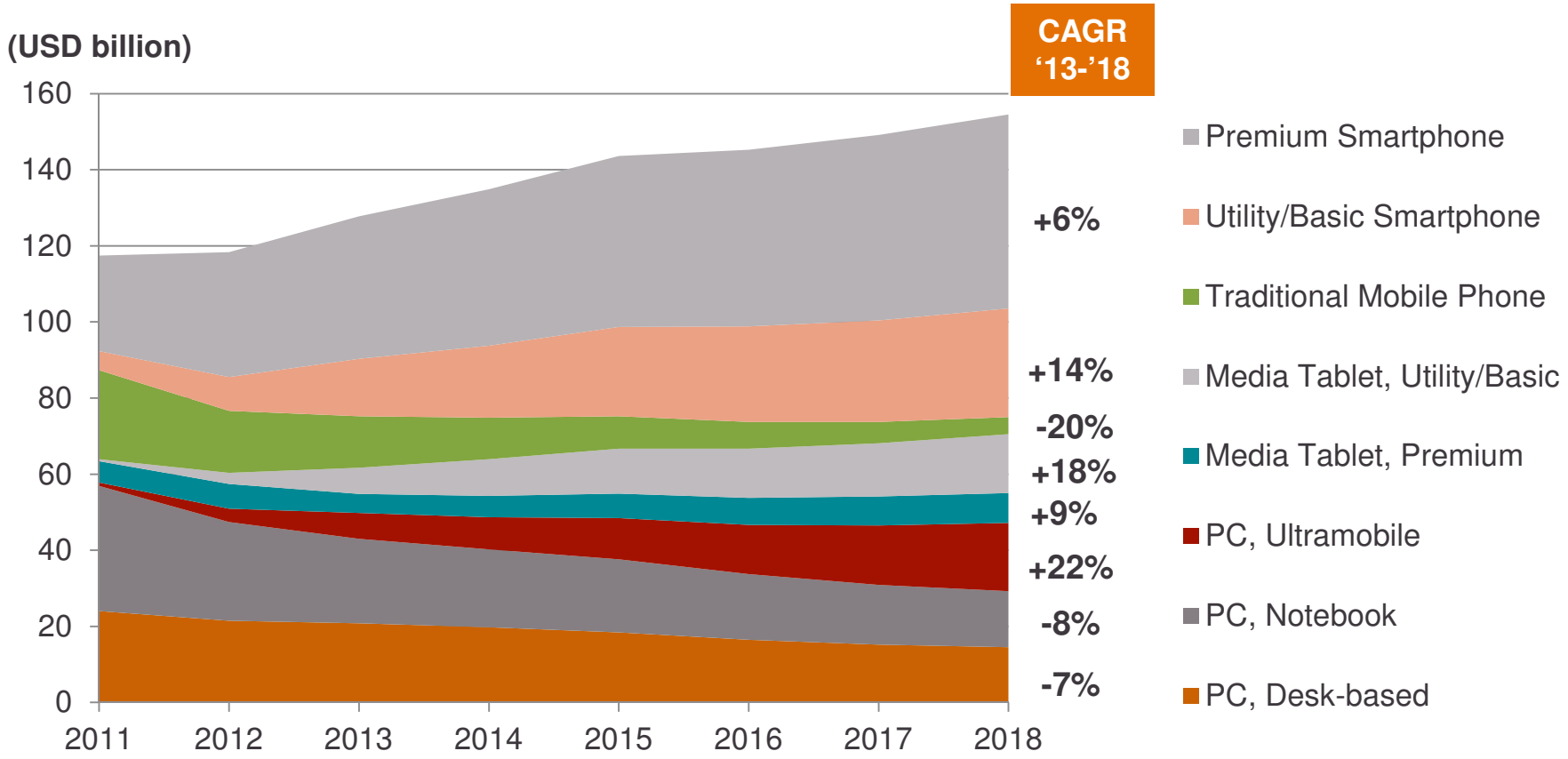


Anisotropic Etch



SEMICONDUCTOR GROWTH DRIVERS

SEMICONDUCTOR SALES BY KEY APPLICATION



Source: Gartner, April 2014

Semiconductor growth drivers are mobile devices
Performance per Watt becoming key metric factor in chip design
Driving further innovation in materials

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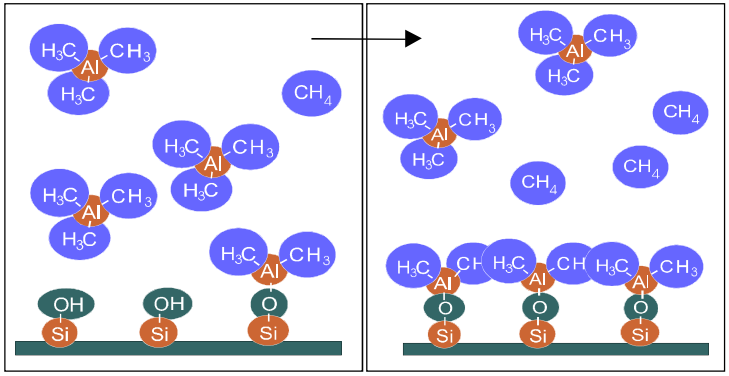
ALD AS AN ENABLER OF NEW MATERIALS

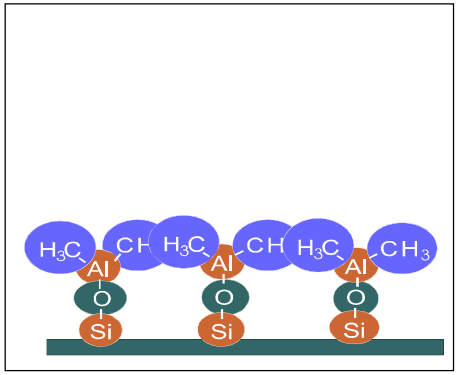
- **New materials and 3D applications require more precise and controlled thin film deposition**

- **Compared to conventional deposition techniques ALD offers superior:**
  - Uniformity
  - Conformality
  - Interface control

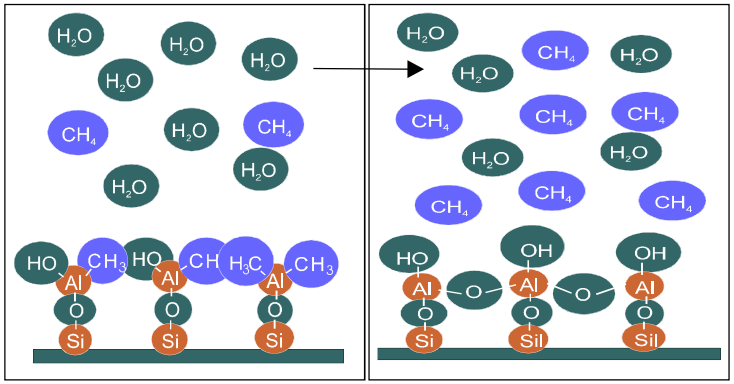
WHAT IS ATOMIC LAYER DEPOSITION (ALD)?



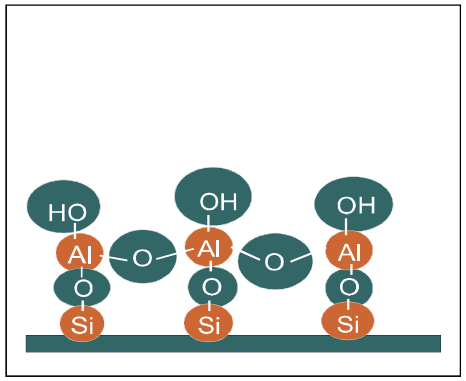
Step 1: (Metal) Precursor Chemi-sorption



Step 2: Purge



Step 3: Reaction to Oxide/Nitride with O_2, H_2O, NH_3 co-reactant



Step 4: Purge

and repeat…

KEY STRENGTHS OF ALD RELATIVE TO CONVENTIONAL DEPOSITION

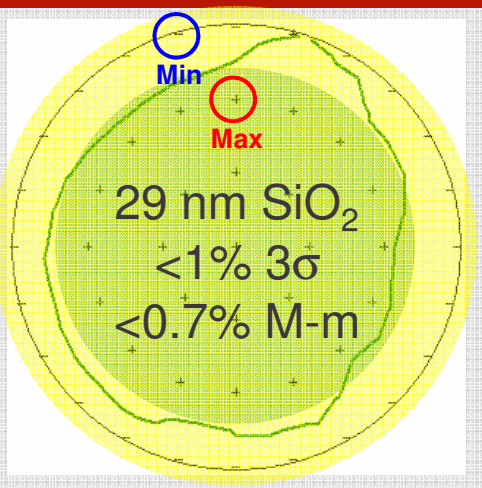
Uniformity

Wafer Statistics

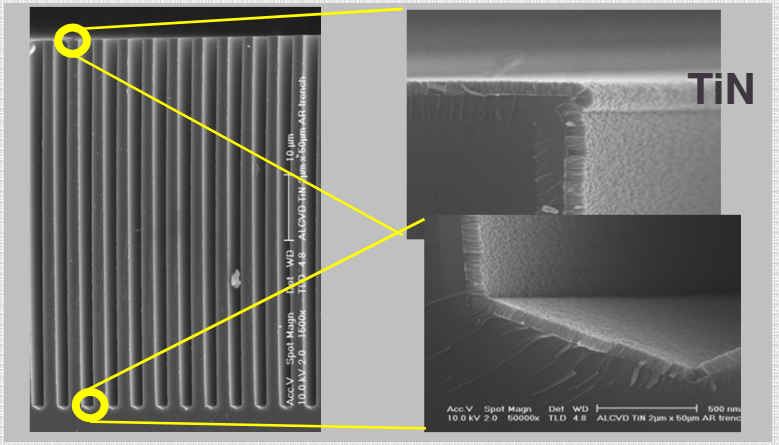
Mean:	291.0183
Maximum:	292.6831
Minimum:	288.7532
Std. Dev:	0.9647908
	0.33 %
Range:	3.9299
Hi/Lo Var:	0.68 %
Unit:	

Wafer Size

Wafer Diam:	300.00 mm
Test Diam:	296.00 mm
No. Sites:	49
Style:	Notch

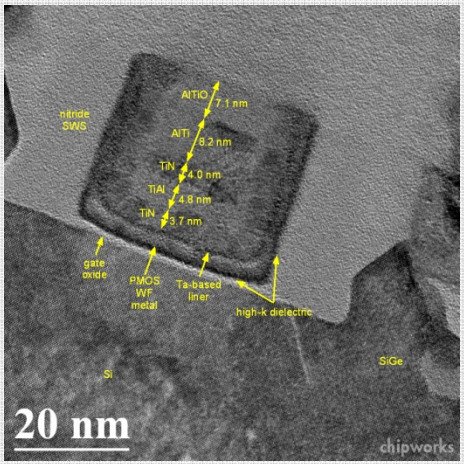


Step Coverage



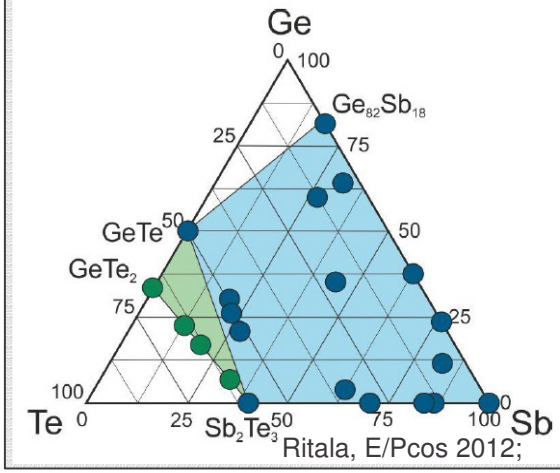
SEM's Courtesy of Philips Research Labs

Interface Control



Atomically engineered interfaces to optimize leakage current, reliability and work-functions

Composition Control



Ritala, E/Pcos 2012;

Excellent composition control for ternary alloys; all ALD solution demonstrated for GST

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ASM AND ALD

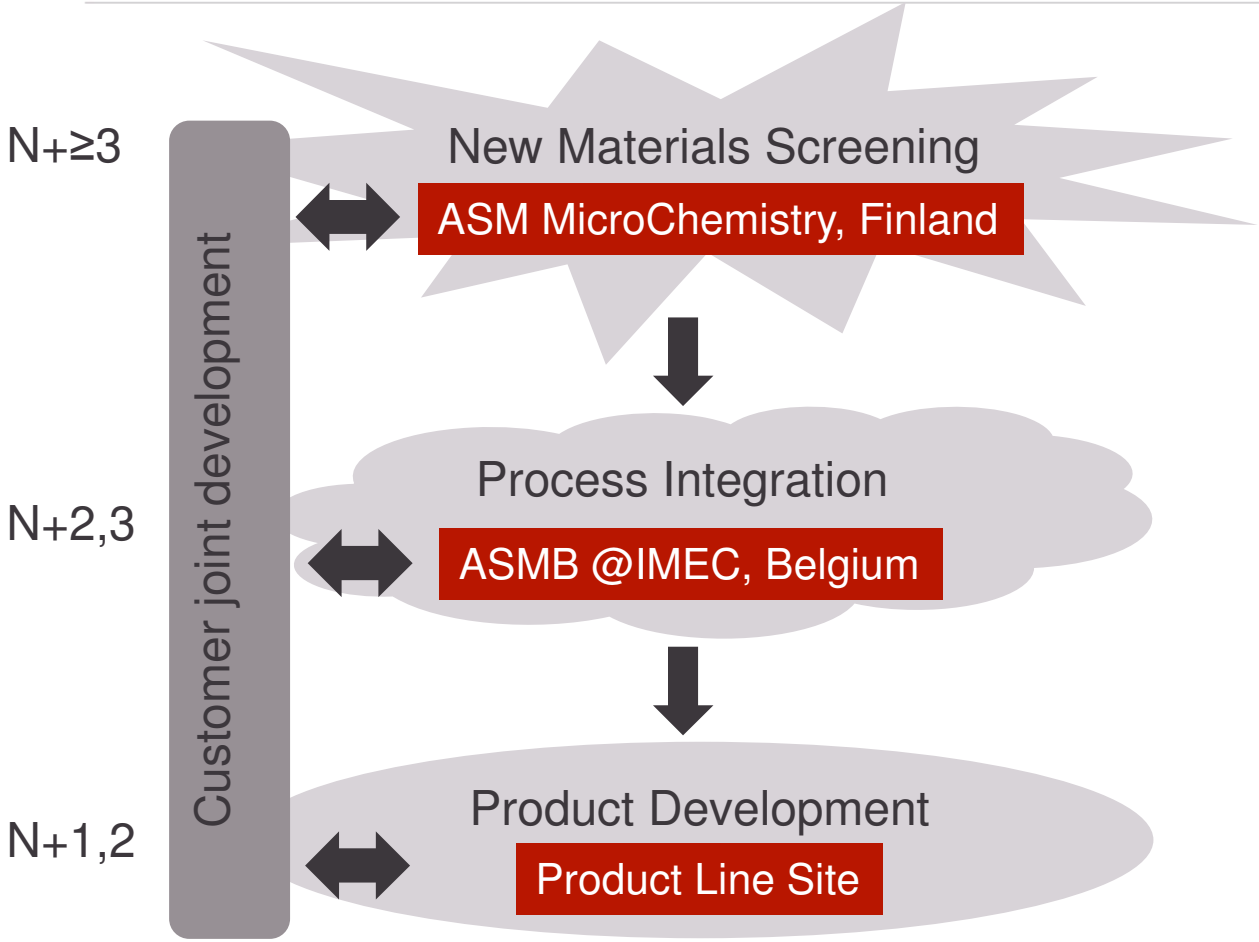
ASM is a leading player in the ALD market

- ASM introduced ALD into the semiconductor market in 1999
- Developing ALD technology since then
- Strong IP position
- Number 1 in high-k gate and strong position in spacer defined double patterning (SDDP)

The ALD market offers strong growth opportunities

- High-k metal gate
- Spacer defined double patterning
- Other emerging applications

ASM NEW MATERIALS DEVELOPMENT STRATEGY



- Basic materials R&D
- Chemical synthesis
- Pre-cursor screening

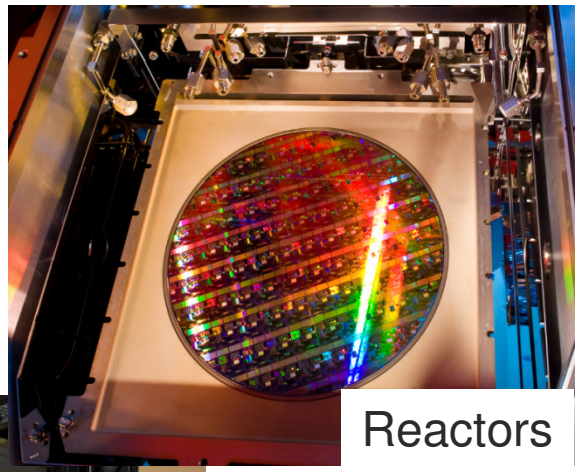
- Process development
- Integration
- Device characterization

- Engineering
- Product development
- Product marketing

CRITICAL ALD SUPPLY CHAIN COMPONENTS

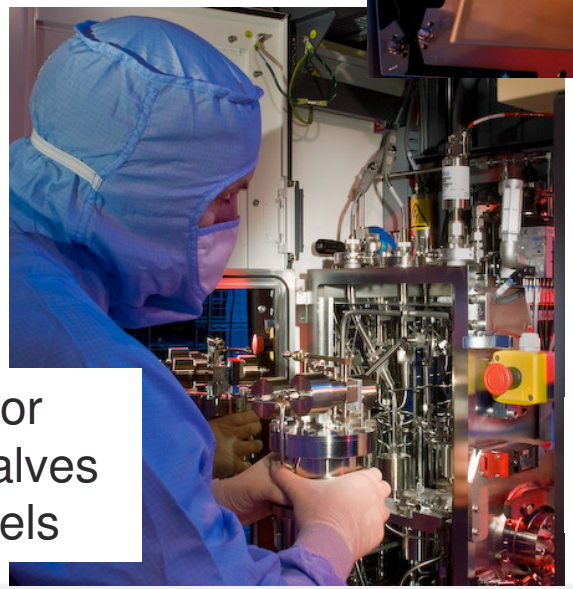
Fundamental Capability → Process Performance → Productivity → Integrated Process → Final Product Capability

Pre-cursors



Reactors

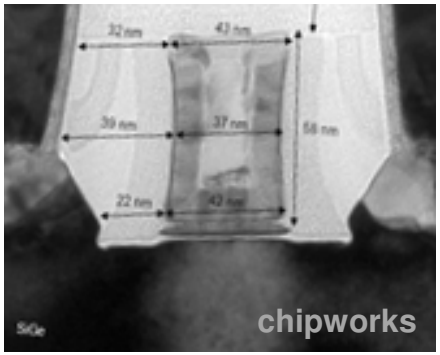
High productivity tools



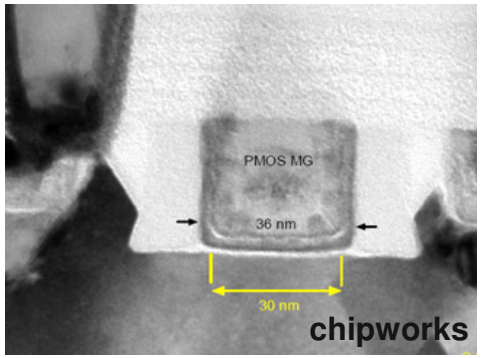
Pre-cursor Delivery, Valves and Vessels

Fab facilities, pumps & abatement

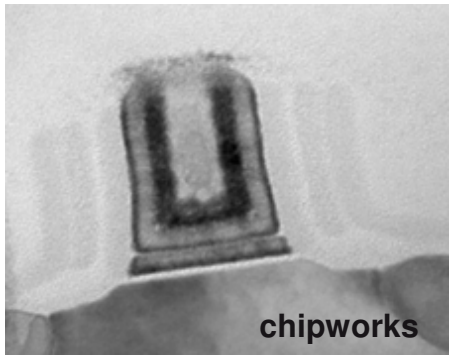
EXTENDIBILITY OF HAFNIUM BASED OXIDES



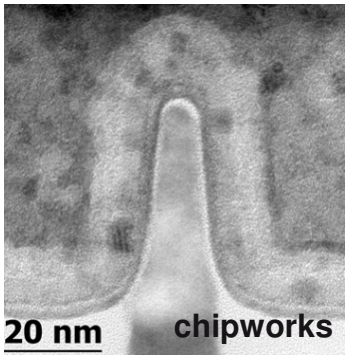
45nm HK first RPMG
Planar FET



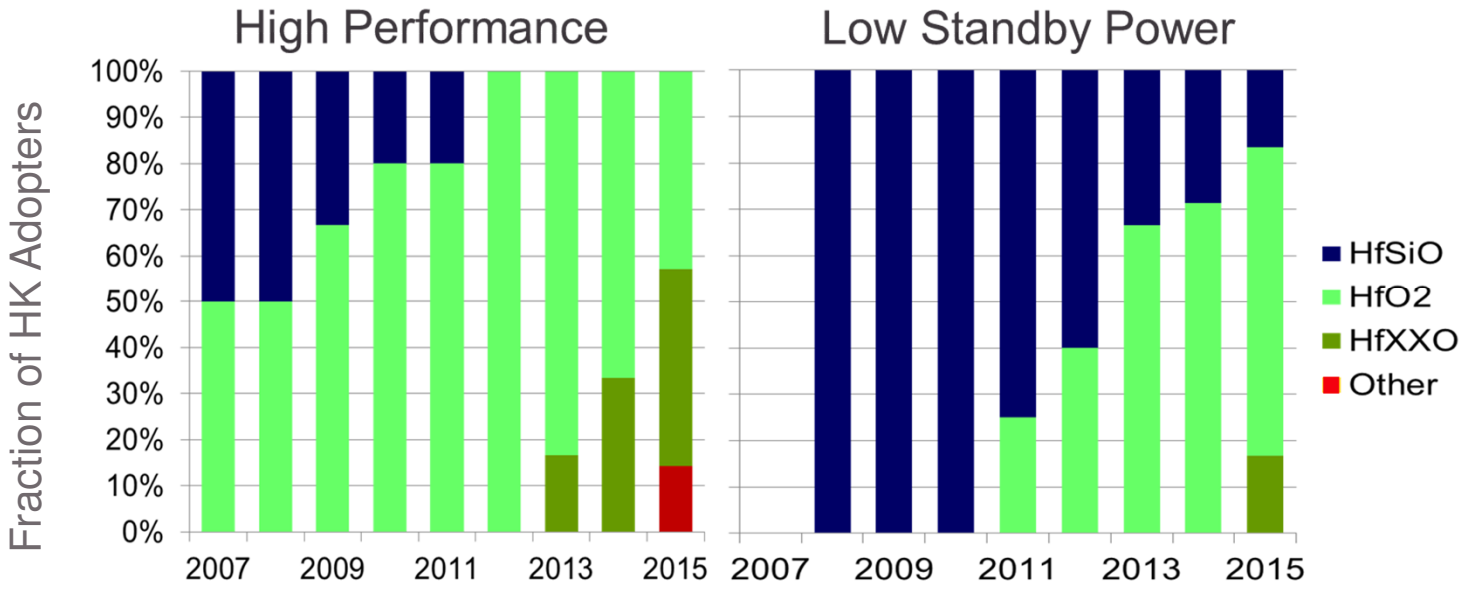
32 nm HK last RPMG
Planar FET



28nm HK first RPMG
Planar FET



22nm HK last RPMG
FinFET



Top: TEM's reproduced with permission of Chipworks
Bottom: ASM estimates 2012

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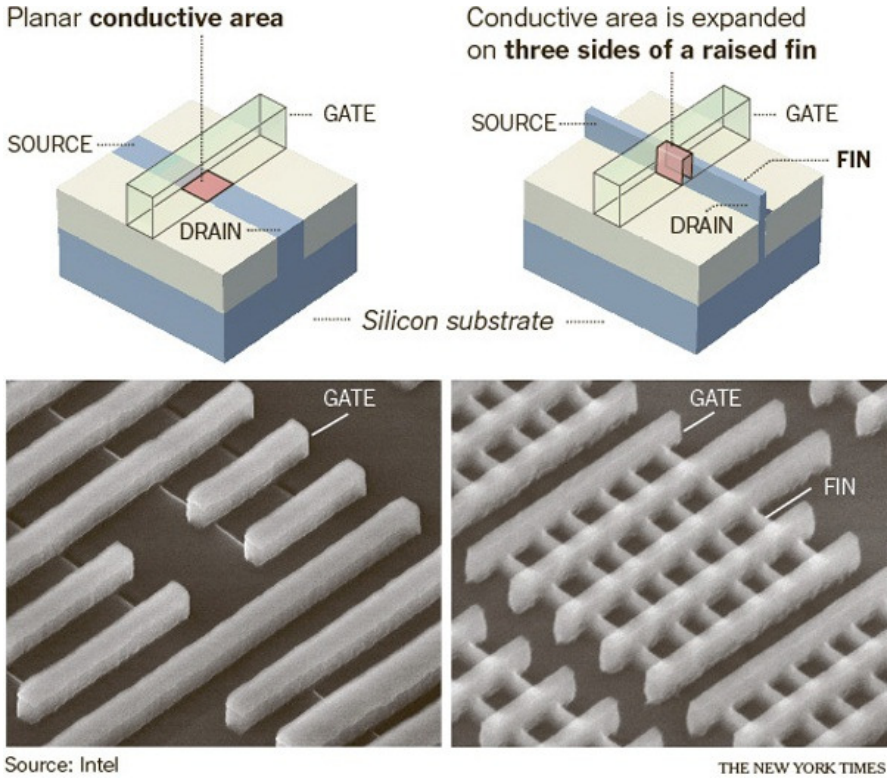
FINFET CHALLENGES:
ALD ENABLES FURTHER SCALING IN 3D



- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- → ALD technology has become critical for HK and MG layers

ASM PRODUCTS
ALD

Pulsar® XP

- ALD for high-k
- Cross-flow reactor
- Solid source delivery system

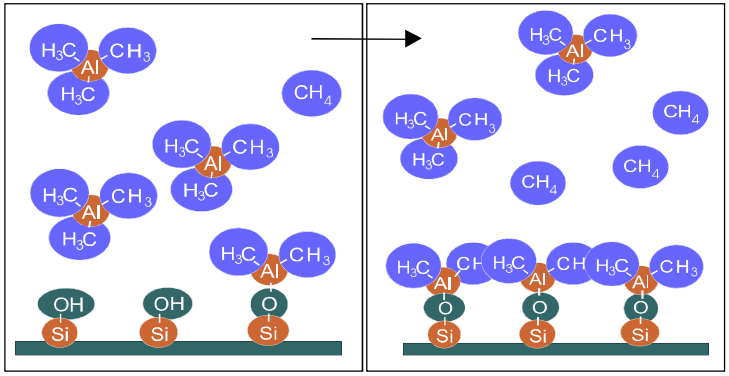
Pulsar® XP

EmerALD® XP

- ALD for metal gates
- Showerhead reactor

EmerALD® XP

WHAT IS PLASMA ENHANCED ATOMIC LAYER DEPOSITION (PEALD)?



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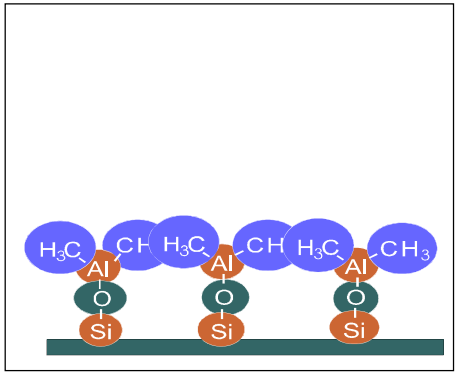
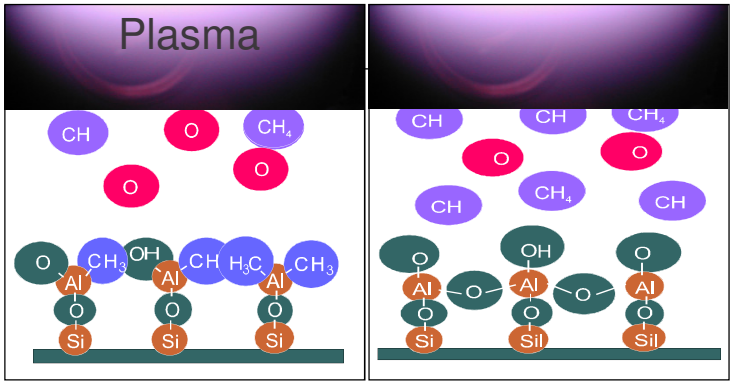
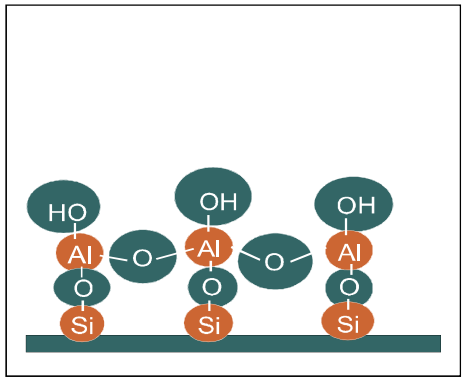


Step 2: Purge



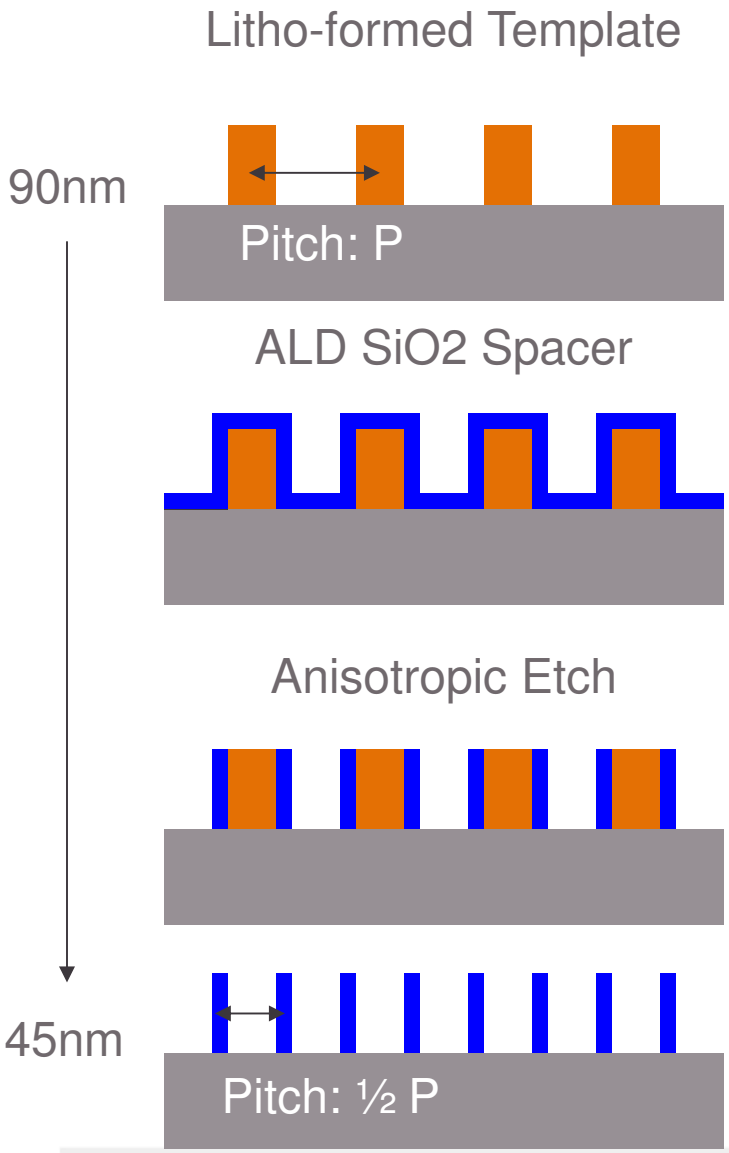
Step 3: Reaction to Oxide/Nitride or metal with O,N,H Radicals

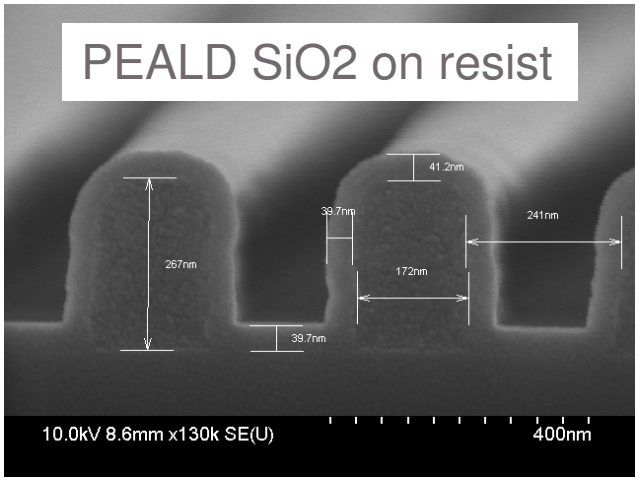


Step 4: Purge

and repeat…

ALD IS ENABLING SUB-RAYLEIGH LIMIT LITHOGRAPHY WITH SPACER DEFINED DOUBLE PATTERNING





Spacer Defined Double Patterning with PEALD in production since 3x nm DRAM and Flash

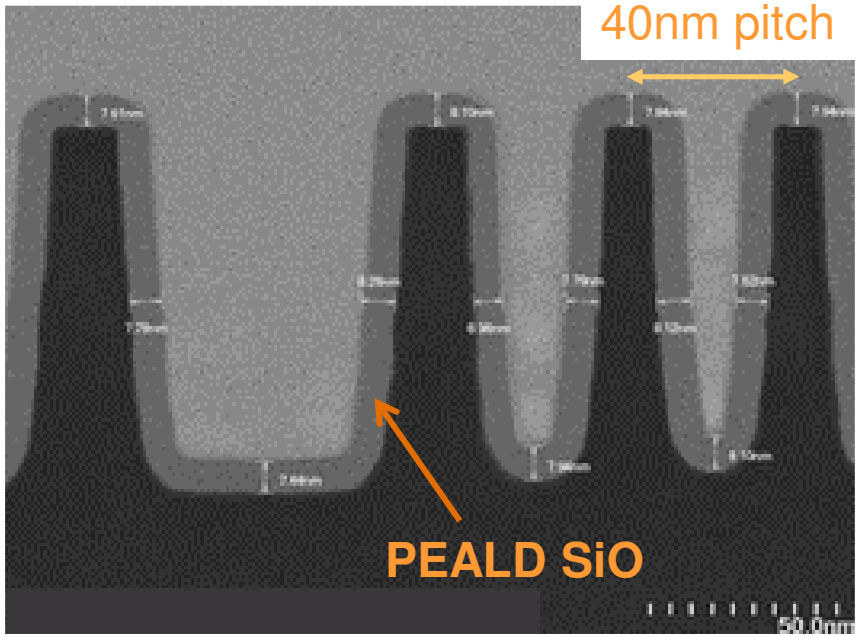
Key enablers brought by PEALD

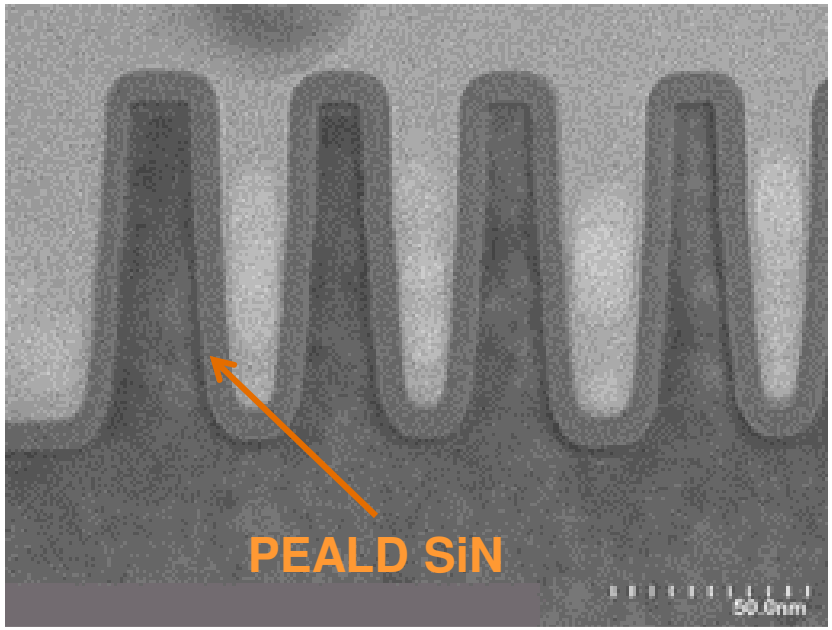
- Uniformity: CD control
- Low temperatures (50C!!)
- Good step coverage
- Dense films
- Extendible to other materials

LINERS AND SPACERS FOR 15 AND 10 nm FinFET'S

PEALD SiO_2 and Si_3N_4 permanent spacers

- Low temperature (300 – 500 °C)
- High conformality
- High quality (low WER, low leakage current)

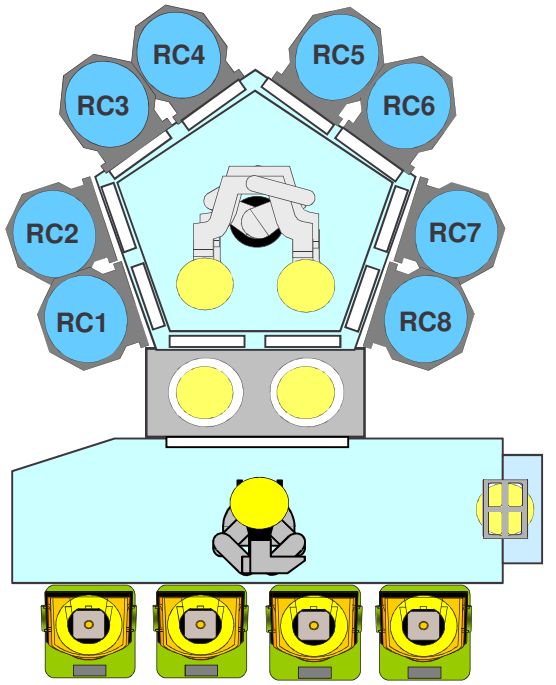




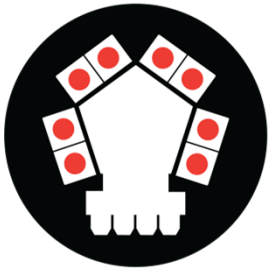
ASM PRODUCTS
PEALD AND PECVD

XP8

- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers for PEALD or PECVD
- PEALD and PECVD can be integrated on the same platform



Eagle® XP8



ASM PRODUCTS

Market Requirements: 22nm→14nm →10nm and beyond

Process	Application	ASM Relative Positioning
ALD and PEALD		
• **ALD solution (Hafnium oxide)**	• ALD key for High-k Metal Gate technology	✓ #1 in the served ALD market
• **PEALD Low temp dielectrics**	• 3D FinFET, GAA require more conformal layers, strength of ALD • SDDP-application of PE-ALD	✓ Qualified by nearly all Logic and Foundry manufacturers ✓ Strengthening inroads with PEALD
Diffusion Furnace	• Traditional materials, such as SiO_2, Si_3N_4, and others are transitioning to ALD and PEALD	
• **Unique "dual reactor dual boat" design**	• Smallest footprint per reactor • Low Cost of Ownership	✓ Leading IC manufacturers are customers
Epitaxy		
• **Epi films for Analog /power devices and for nMOS & pMOS transistors (logic & memory)**	• Thick Epi layers for power devices • Strained & relaxed Epi films for planar & FinFET devices	✓ ASM one of only two top vendors
PECVD		
• **Extreme low-k films**	• Advanced intermetal dielectric film	✓ ASM one of only two top vendors in PE-CVD low-k

Strong IP protected portfolio

ASM PRODUCTS
ADVANCED EPITAXY

Advanced transistors enabled with Intrepid® XP

- Strained epitaxial films for planar logic devices
- Relaxed & strained epitaxy for Si, SiGe & Ge based FinFETs through 7nm
  - Channel (SRBs), S/D stressor, contact & passivation cap layer

Integrated, low thermal budget pre-clean module

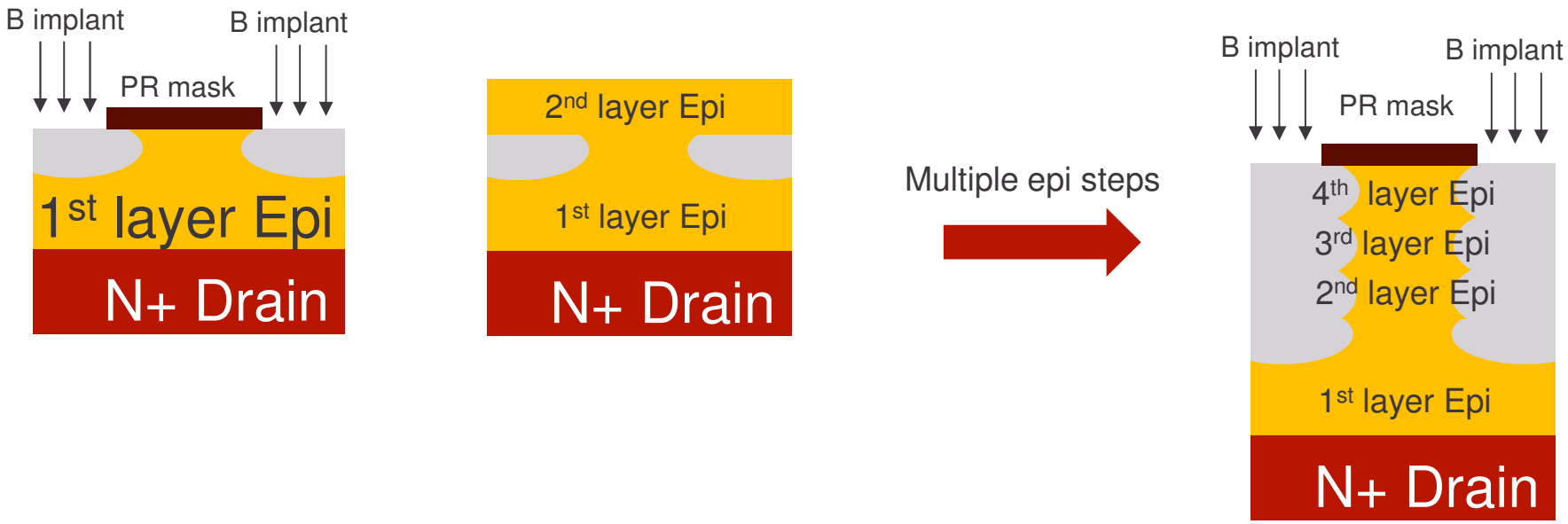
- High quality surface with low interface contamination

High productivity & lowest CoO

- Platform capability with 4 process modules
  - Flexible configuration with pre-clean (3+1& 2+2)
- Differentiated film growth processes enabling devices with high drive currents & best-in-class productivity
- High throughput with pulsed Epi processes & high doping levels

Intrepid® XP

EPI LAYERS FOR POWER DEVICES
MULTI-LAYER EPI TECHNOLOGY



- **Power devices require multiple & thick Epitaxial films to withstand high breakdown voltages (600V ~ 800V)**
- **Breakdown voltage of the device dictates number of Epi layers needed**
- **In HVM by several power device manufacturers enabled by:**

ASM Product: Epsilon® 3200

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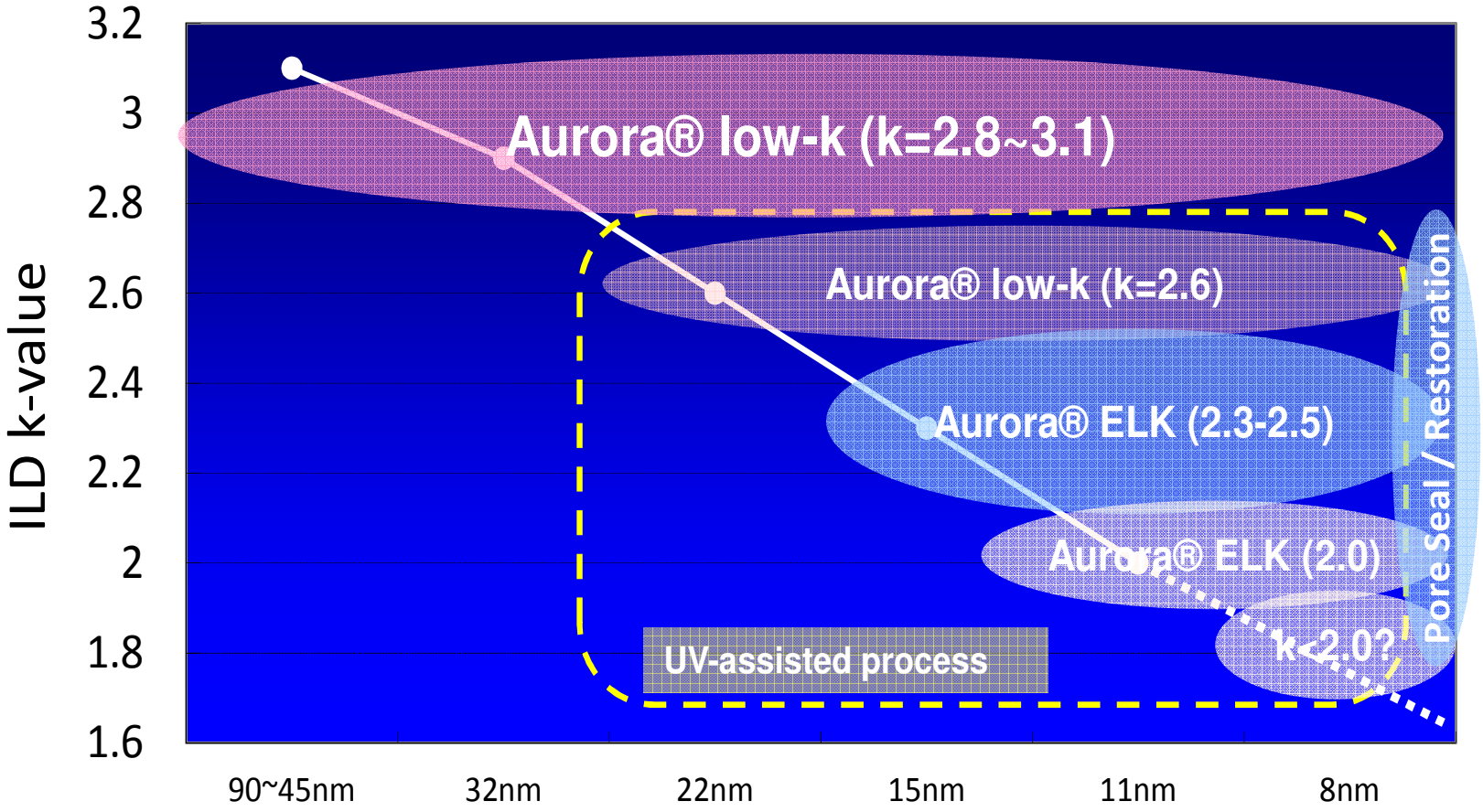
ALD and PEALD		
• **ALD solution (Hafnium oxide)**	• ALD key for High-k Metal Gate technology	✓ #1 in the served ALD market
• **PEALD Low temp dielectrics**	• 3D FinFET, GAA require more conformal layers, strength of ALD	✓ Qualified by nearly all Logic and Foundry manufacturers
	• SDDP-application of PE-ALD	✓ Strengthening inroads with PEALD
Diffusion Furnace	• Traditional materials, such as SiO_2, Si_3N_4, and others are transitioning to ALD and PEALD	
• **Unique "dual reactor dual boat" design**	• Smallest footprint per reactor	✓ Leading IC manufacturers are customers
	• Low Cost of Ownership	
Epitaxy	• Thick Epi layers for power devices	✓ ASM one of only two top vendors
• **Epi films for Analog /power devices and for nMOS & pMOS transistors (logic & memory)**	• Strained & relaxed Epi films for planar & FinFET devices	
PECVD		
• **Extreme low-k films**	• Advanced intermetal dielectric film	✓ ASM one of only two top vendors in PE-CVD low-k

Strong IP protected portfolio

EXTENDIBILITY OF ASM'S LOW-K SOLUTION



ASM PRODUCTS

Market Requirements: 22nm→14nm →10nm and beyond

Process	Application	ASM Relative Positioning
ALD and PEALD		
• **ALD solution (Hafnium oxide)**	• ALD key for High-k Metal Gate technology	✓ #1 in the served ALD market
• **PEALD Low temp dielectrics**	• 3D FinFET, GAA require more conformal layers, strength of ALD	✓ Qualified by nearly all Logic and Foundry manufacturers
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PECVD		
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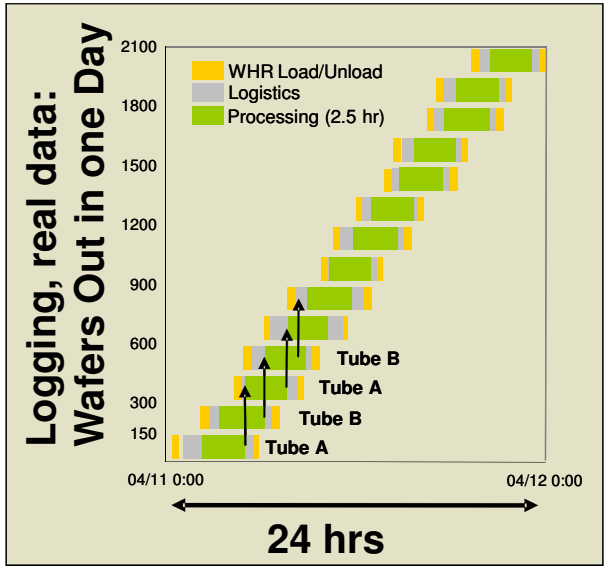
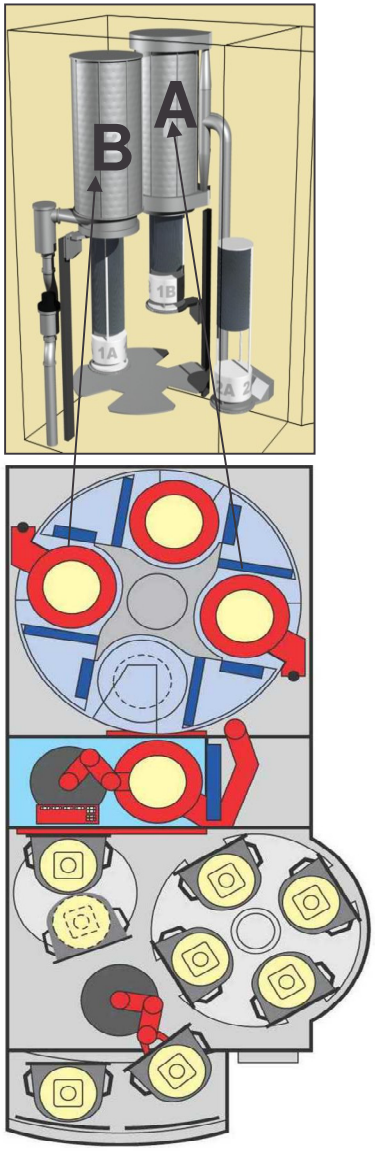
Strong IP protected portfolio

PRODUCTIVITY AND INNOVATION

Productivity

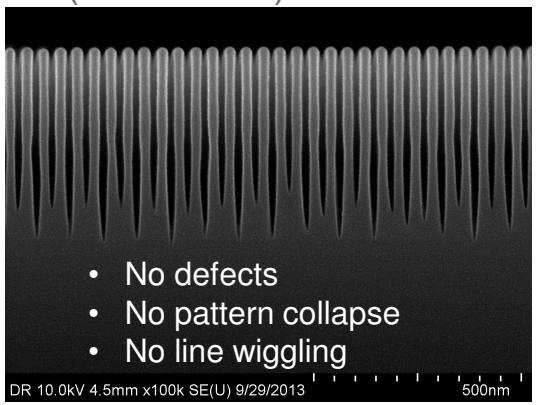
- One A412 PLUS = > 80 kwpm (example: 2.5 hr process, 95% available, 150 product wafer load)
- Dual boat/dual reactor system
- Clustering between reactors possible – only vertical furnace in the market with this capability



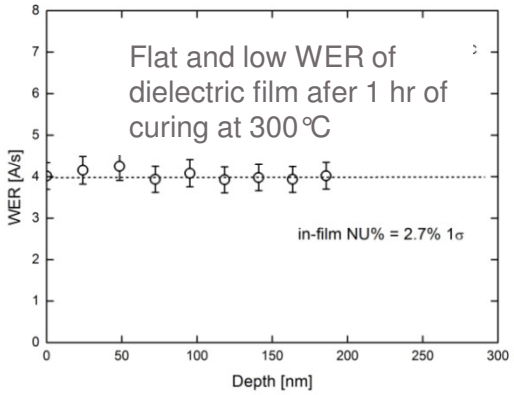


Innovation: novel processes

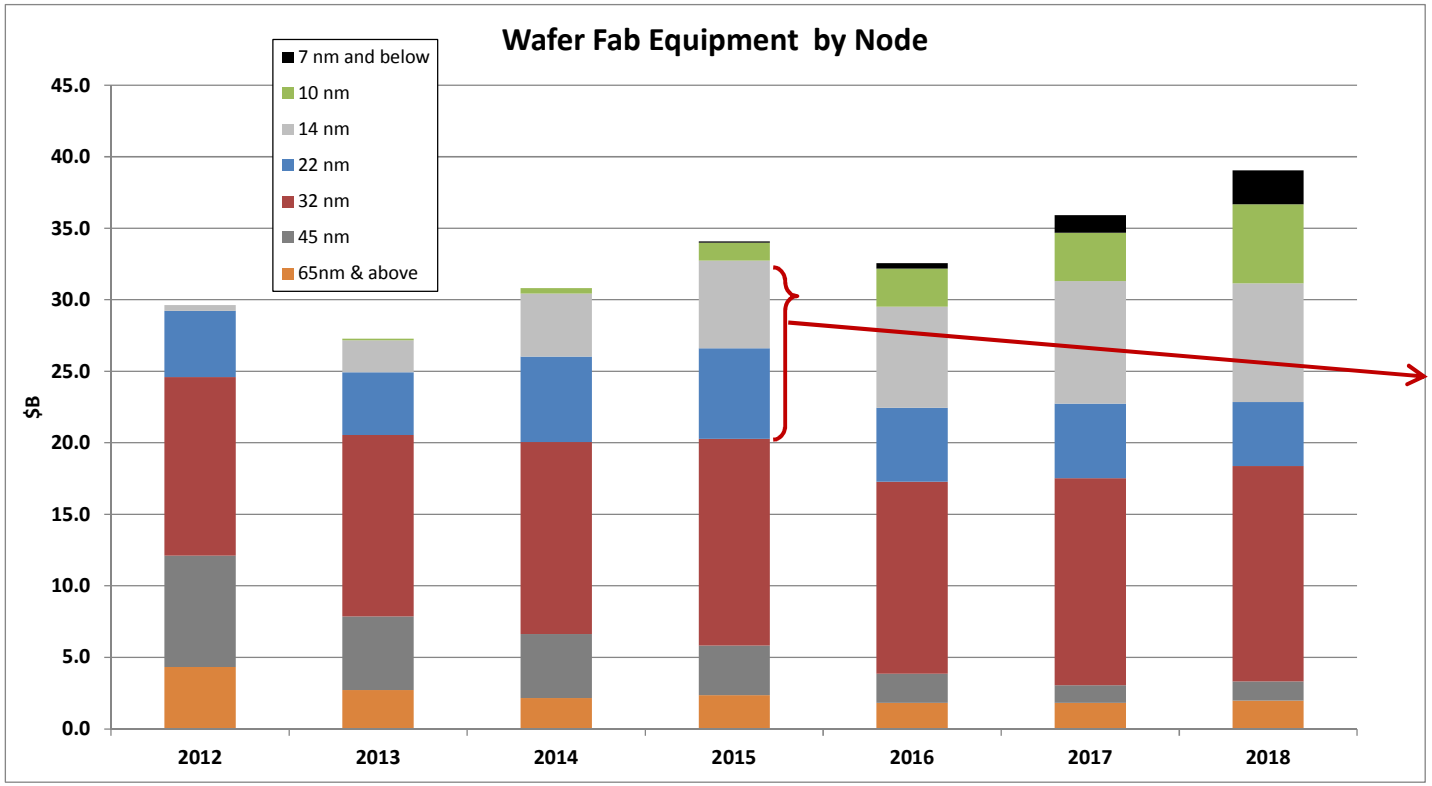
- Example 1: Novel hard mask materials – e.g. for fabrication of high aspect ratio structures in silicon (with IMEC)



- Example 2: Low temp reactive curing of dielectric film (WER 5A/s)



WAFER FAB EQUIPMENT FORECAST



Share of 22nm and 14nm of total Equipment spending increasing in 2014-2015

Gartner April, 2014

Key customer ALD and PEALD penetrations in 22nm and 14nm: market segments with high expected growth

OUTLINE

- **New Materials: Moore's law enablers**
- **ALD as enabler of new materials**
  - What is Atomic Layer Deposition (ALD)?
  - Key strengths of ALD
- **ASM and ALD**
- **ASM Products and selected applications**
- **Summary and Conclusions**

SUMMARY AND CONCLUSIONS

- Scaling is increasingly enabled by new materials and 3D technologies
- ALD and PEALD enable new materials and 3D
- The ALD market offers strong growth opportunities
- Intrepid® XP, system with 4 Epi reactors, targeting strained Epi layers for CMOS, and Epsilon® 3200 for analog/power
- ASM's low-k technology continues to be extendible
- ASM's Vertical Furnace is providing high productivity, in combination with continued process innovation

DRIVE INNOVATION • DELIVER EXCELLENCE