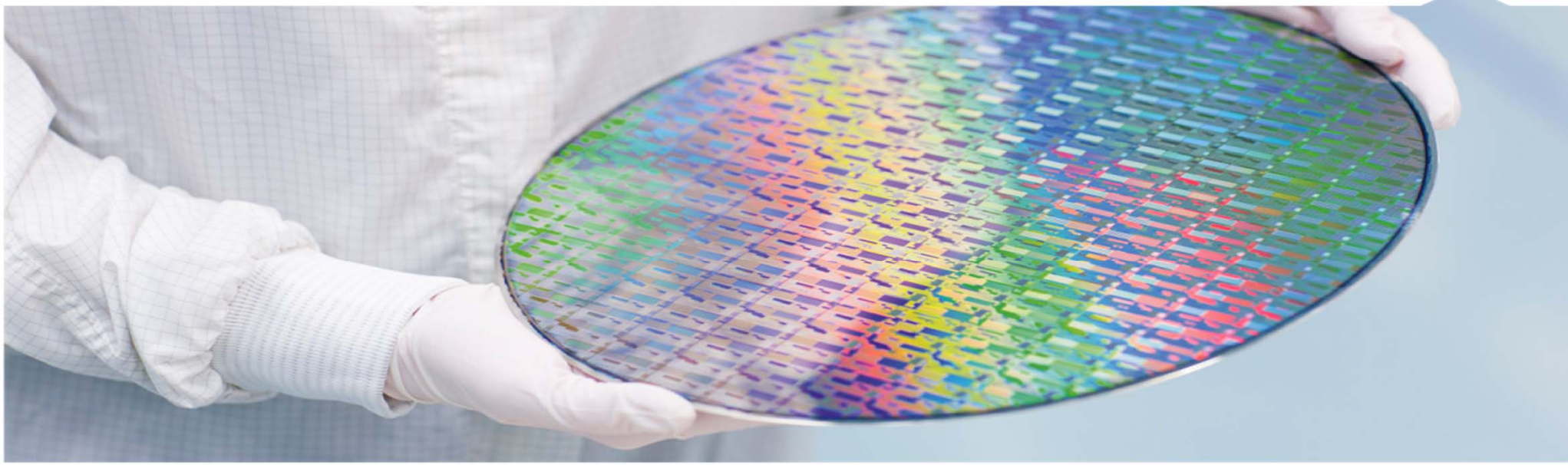
DRIVE INNOVATION · DELIVER EXCELLENCE



ENABLING ADVANCED WAFER PROCESSING WITH HIGH PRODUCTIVITY SYSTEMS AND NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 9, 2019

CAUTIONARY NOTE

Cautionary Note Regarding Forward-Looking Statements: All matters discussed in this presentation, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholders or other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's reports and financial statements. The Company assumes no obligation nor intends to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **Device and Technology trends driving the ALD market**
  - Logic
  - Memory
  - Patterning
- **ALD**
  - ASM ALD Products
  - Selected applications in Logic, 3D-NAND, DRAM and Emerging Memory
- **PECVD**
- **Vertical Furnace**
- **Epitaxy**
  - Epi process applications
  - Intrepid ES features and benefits
- **Epitaxy – Introducing Previum®**
  - Previum® features & benefits

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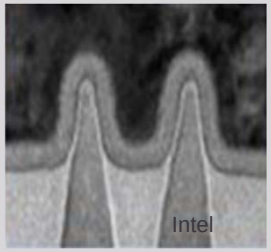
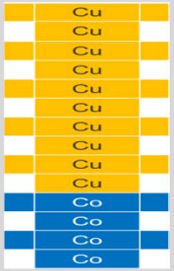
DEVICE AND TECHNOLOGY TRENDS DRIVING ALD MARKET

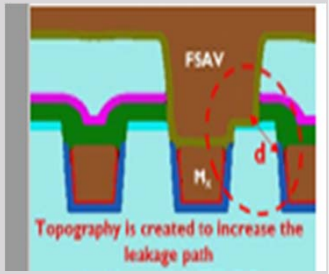
Logic

FinFET → Gate All Around



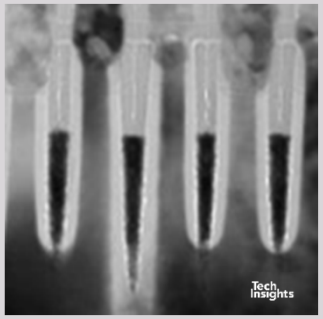


New Conductors

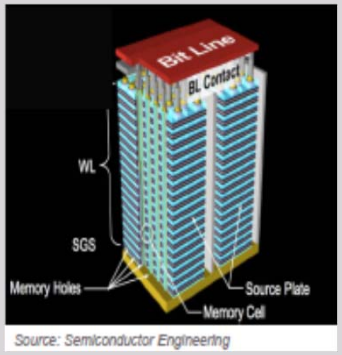


Selective Deposition

Memory



New metal for buried WL



Source: Semiconductor Engineering

Emerging Memory

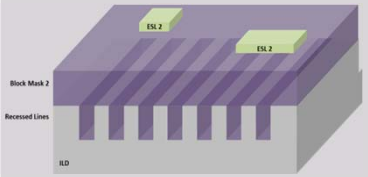
PCRAM - Chalcogenides

ReRAM

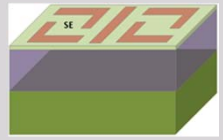
FeRAM

CBRAM

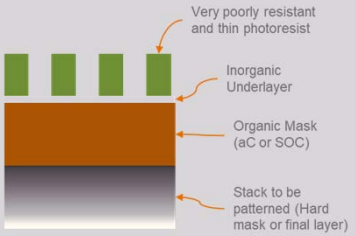
Patterning



Gap fill for Self-aligned Blocks

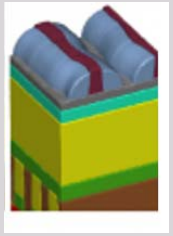


EUV SE



Source: Imec, public

EUV Underlayers



https://semiengineering.com/photoresist-shape-in-3d/

EUV SDDP

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ASM PRODUCTS
ALD (I)

EmerALD®

Pulsar®

Synergis®

ASM PRODUCTS
ALD (II)

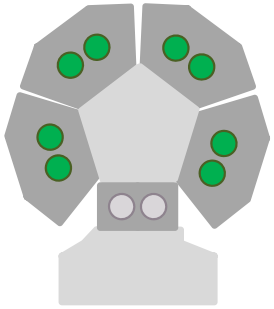
- Introduced **Synergis®** in 2018
- New dual chamber thermal ALD reactor technology evolved from decades of **ALD expertise** on Pulsar and EmerALD
- Leverages industry proven XP8 platform architecture for **high productivity** solutions for logic and memory applications while maintaining **single wafer process control**
- Highly **flexible** source layout including ASM's proven **solid source delivery** technology
- Ability to run clustered processes with **high tool availability** to lower overall cost per wafer

SYNERGIS® COMBINES KEY ALD TECHNOLOGIES

Single Wafer

Clustering
Process Flexibility
High Productivity

Synergis®



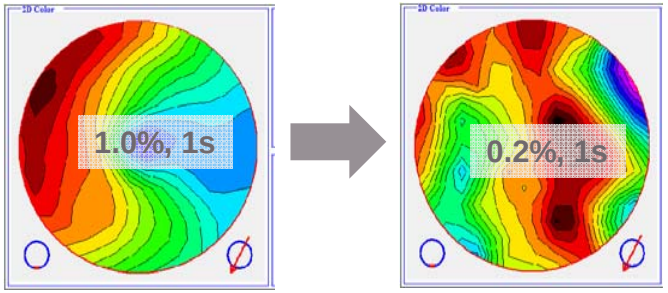
Synergis®

› **Designed for optimal ALD performance:**

1. **Improve wafer thermal uniformity**
2. **Delivery of multiple low and high vapor pressure precursors for process flexibility**
3. **Manufacturability – Short PM Time & High Throughput**
4. **Reduced reactor volume and improve purge efficiency**

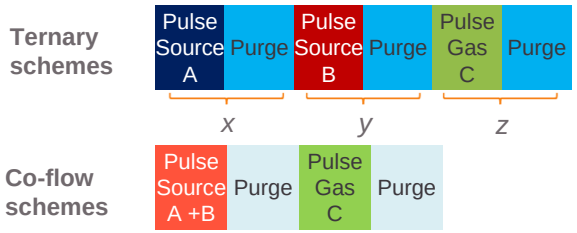
SYNERGIS® INNOVATIONS FOR FLEXIBILITY AND PERFORMANCE

THERMAL UNIFORMITY



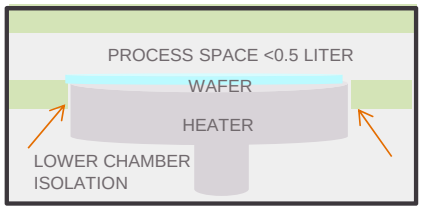
Improved WIWNU performance through thermal optimization

FLEXIBLE PRECURSOR DELIVERY



Ternary and complex doped films with infinitely flexible pulsing schemes

PURGE EFFICIENCY

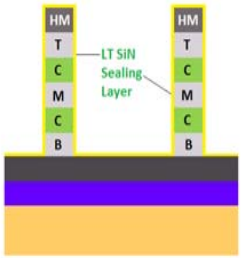


True ALD performance with small reactor volume & high flow purge circuits

HIGH TOOL AVAILABILITY

Reduced PM times with fast switch-out reactor PM modules

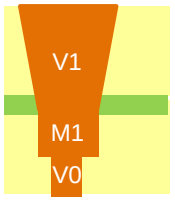
SYNERGIS® ADDRESSES THE EXPANDING ALD APPLICATION SPACE



Low temperature, low-k encapsulation and hermetic sealing layers

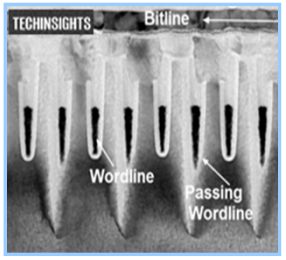
DX

MX



~1nm metal oxide ESL

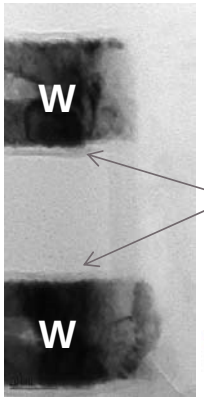
Metal oxide hard masks and etch stop layers with tunable etch properties



ML

Low resistivity pure metal layers for DRAM and 3D-NAND word line

NT



Low resistivity, ultra-thin enhanced barrier solutions for logic and memory

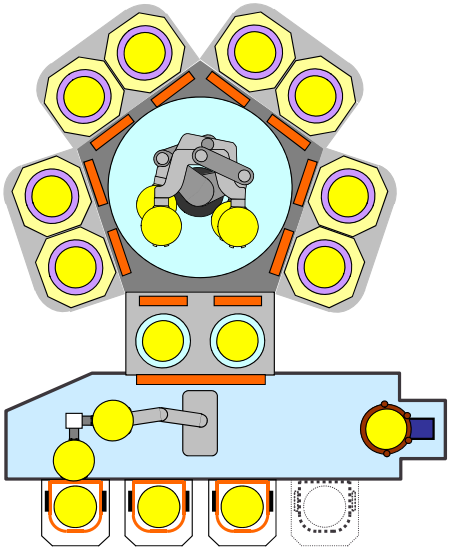
SYNERGIS® ALD: HIGHEST PERFORMANCE AT THE LOWEST COST PER WAFER

- **Synergis® thermal ALD provides best productivity without sacrificing film performance**
  - Significant reduction in capital costs and fab footprint
- **Flexible platform and architecture to meet needs of sub-7 nm technologies**
  - Ability to deposit metal oxides (MX), metal nitrides (NT), dielectrics (DX) and pure metals (ML)
- **Adopted for multiple applications at logic and memory customers with proven HVM readiness**
  - Many applications currently under development

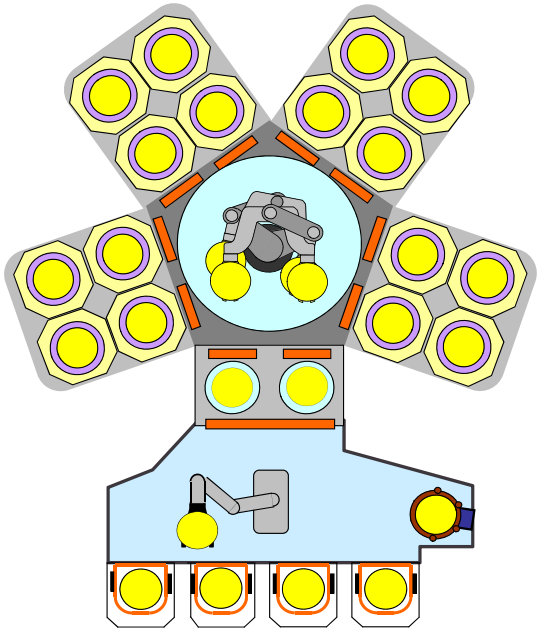
ASM PRODUCTS
PEALD AND PECVD

XP8® -DCM / QCM

- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers for DCM, 16 chambers for QCM
- PEALD and PECVD can be integrated on the same platform



DCM (Dual Chamber Module)



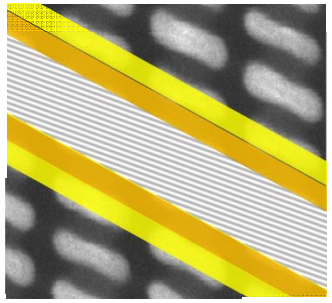
QCM (Quad Chamber Module)

PATTERNING SPACER APPLICATIONS

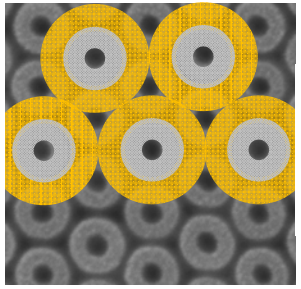
Photo Source: TechInsights

DRAM (1X)

Multiple patterning spacers examples



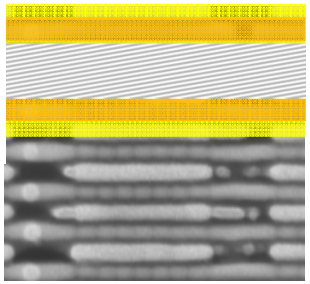
Active STI/Gate(SDQP)



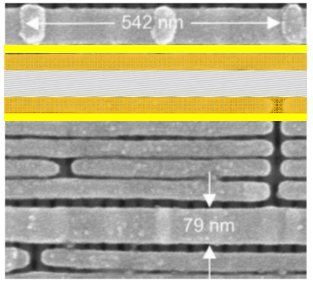
Storage Node (SDDPx2)

Logic (10~5nm)

Multiple patterning spacers examples



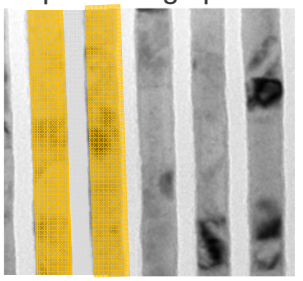
Fin/Gate Formation (SDQP)



M0~M1 (SDQP)
M2~M5(SDDP)

3D-NAND

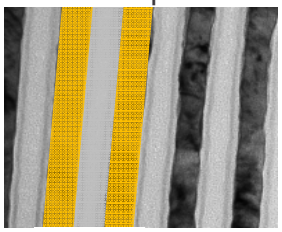
1patterning spacer



Bit Line (SDDP)

Emerging Memory

Multiple patterning spacers examples



Bit Line (SDDP)
Word Line (SDDP)

The most critical spacers may require “EUV + SDDP” integration in near future

PEALD PROCESSES FOR LOGIC APPLICATIONS

PEALD application

Photo Source: TechInsights

Cut Mask Gap-fill

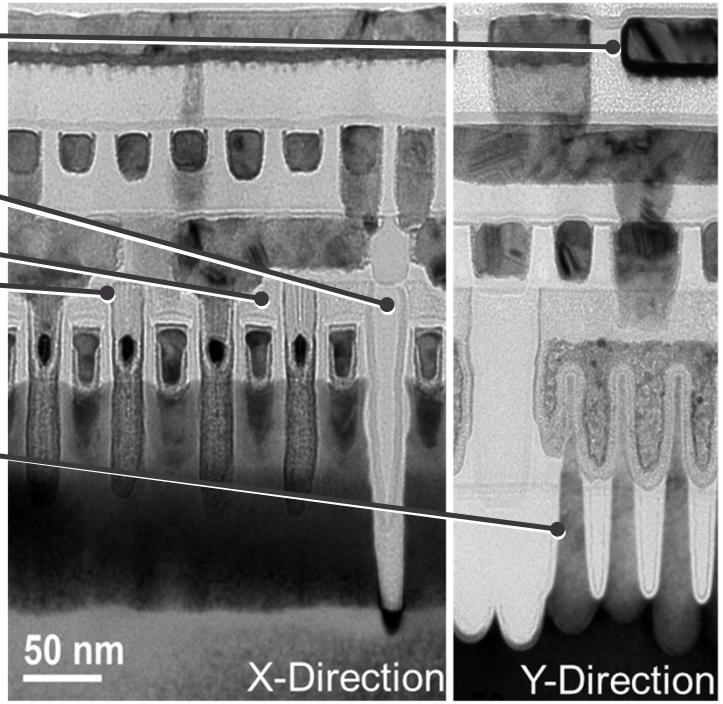
SDB Gap-fill

COAG SAC Gap-fill

IO Transistor Gate Oxide

Solid state doping

Patterning HM



COAG : Contact on Active Gate
SDB : Single Diffusion Break
SAC : Self Align Contact

- Maintaining POR position in oxide layers. Adding high quality oxide
- Device shrinkage increases demand for PEALD layers

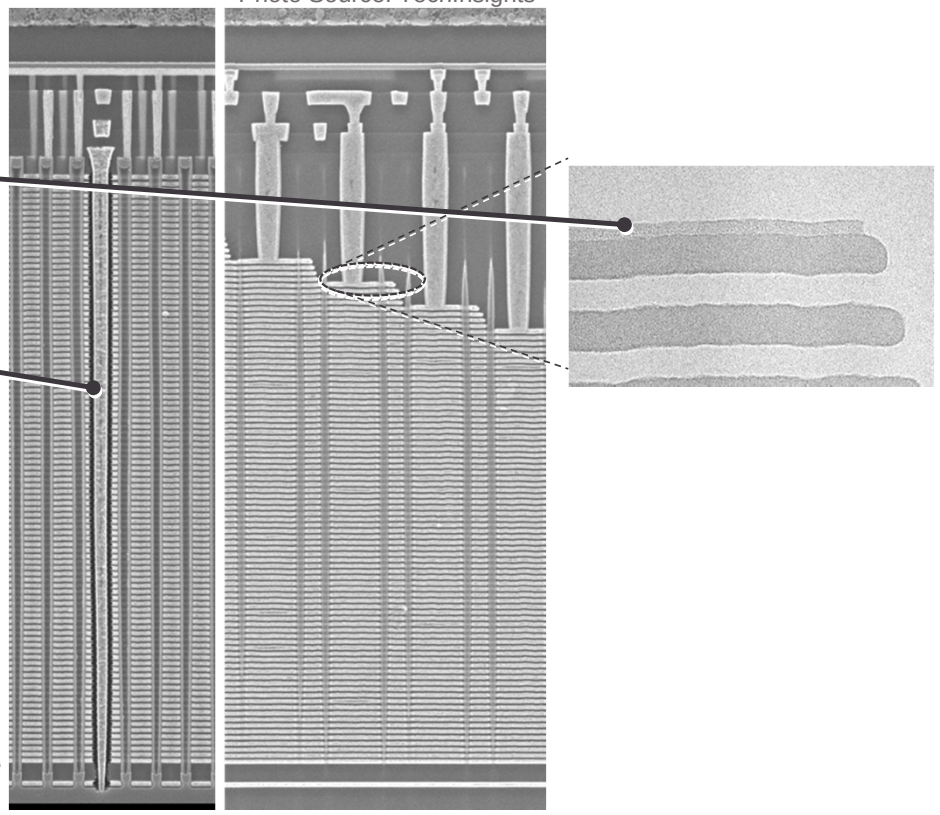
PEALD PROCESSES FOR 3D-NAND APPLICATIONS

PEALD application

Photo Source: TechInsights

Raising Contact Landing Pad

Slit Oxide Liner

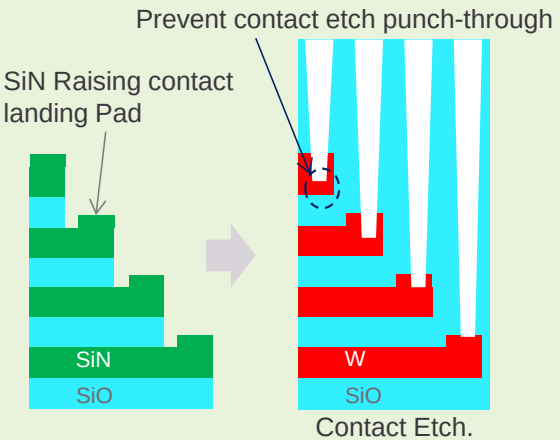


92 stack 3D-NAND device

- High aspect structure requires conformal film by using high coverage PEALD

PEALD SiN FOR 3D-NAND APPLICATIONS

Raising Contact Landing Pad by PEALD SiN



Samsung VLSI Symp 2009

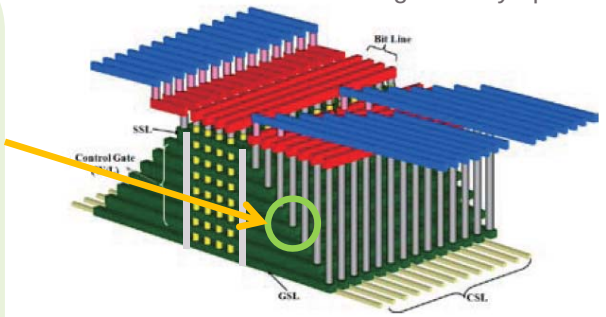
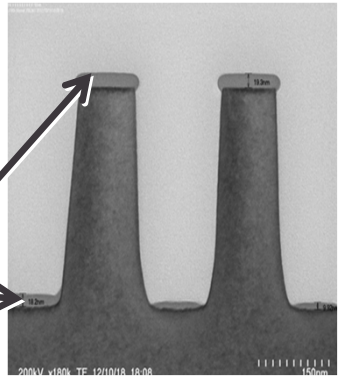
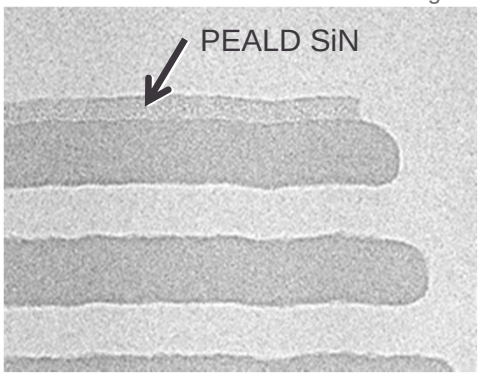


Photo Source: TechInsights





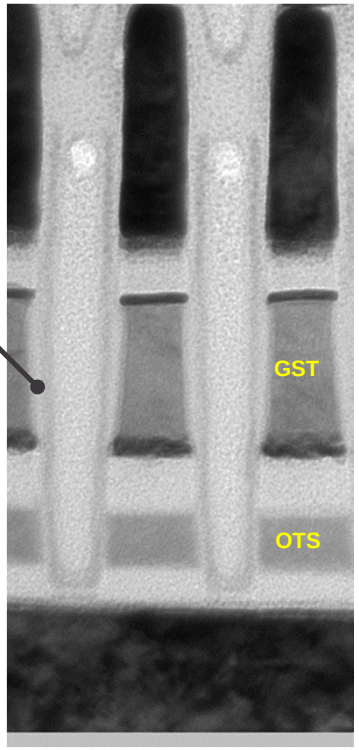
- PEALD SiN
  SiN film on Top and Bottom only

- Fewer etch steps and more process latitude to create staircase

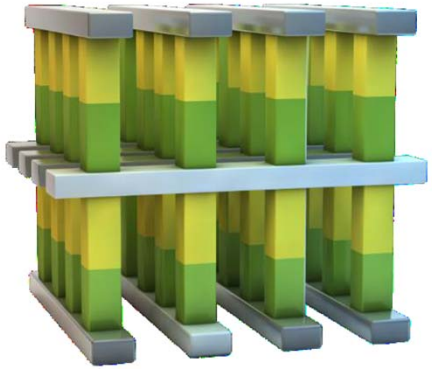
PEALD PROCESSES FOR EM APPLICATIONS

PEALD application

GST inner liner



Source:TechInsights



Source:Micron

- As GST chalcogenide has low resistance to heat, PEALD / PECVD which enables low temperature film deposition is widely used.

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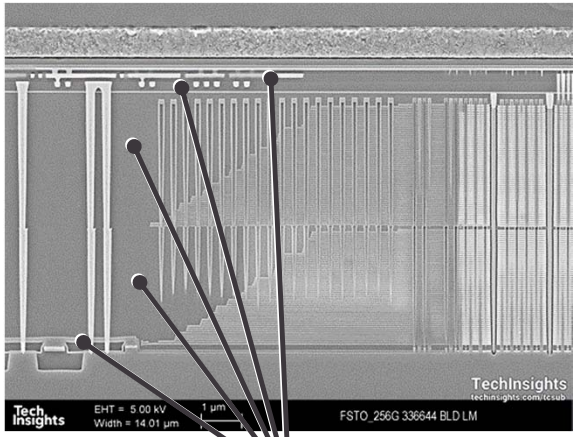
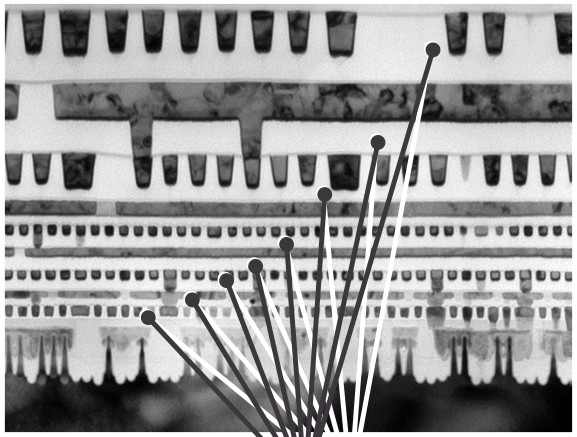
PECVD PROCESS APPLICATIONS

Photo Source: TechInsights



TEOS
- High throughput
- Good wiw uniformity
- High quality
- Stress control

Photo Source: TechInsights



BEOL Low-k
- High throughput
- Good wiw uniformity
- High EM: direct CMP
- No need for glue layer
- Stress control

- Growing PECVD SAM in 3D-NAND, logic, DRAM and CIS

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ASM PRODUCTS
FURNACE LPCVD /DIFFUSION /BATCH ALD

A412™

- Dual boat/dual reactor system
- Clustering of applications between reactors possible – only vertical furnace in the market with this capability
- Up to 150 product wafer load size

A400™ for More than Moore Devices

- Dual boat/dual reactor system
- Simultaneous handling of Dual size wafers
- Up to 150 product wafer load size

Applications:

- Full range of applications for Logic, Memory, Power, Analog/RF and MEMS Devices

- LPCVD Silicon, SiN, TEOS, HTO
- Diffusion, Anneal, Cure, Reactive Cure
- Batch ALD (AlO, AlN, TiN, SiN, SiO, etc)

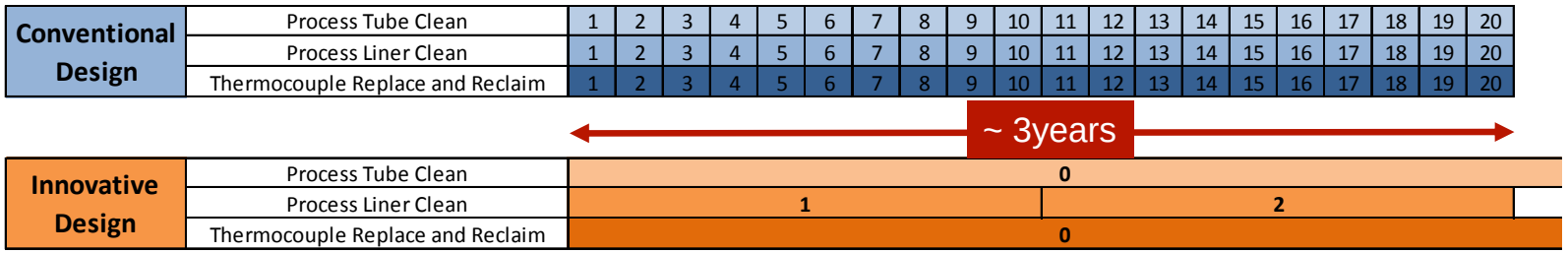
Example: LPCVD Silicon with Ultra long Preventive Maintenance Cycle

- LPCVD Si process applications
  - UNDOPED films
  - DOPED (P,B) films
- Growing Si Power device market
- Driven by Automotive and Industrial Electronics

- This technology enables low Total Cost of Ownership (TCO) for Si Power IGBT and MOSFET devices manufacturing

Process Tube stays clean: No deposition

Preventive Maintenance item	Conventional Design	Innovative Design
	Deposited thickness LPCVD Si	Deposited thickness LPCVD Si
Process Tube Clean	@50 µm	None
Process Liner Clean	@50 µm	@500 µm
Thermocouple Replace and Reclaim	@50 µm	None



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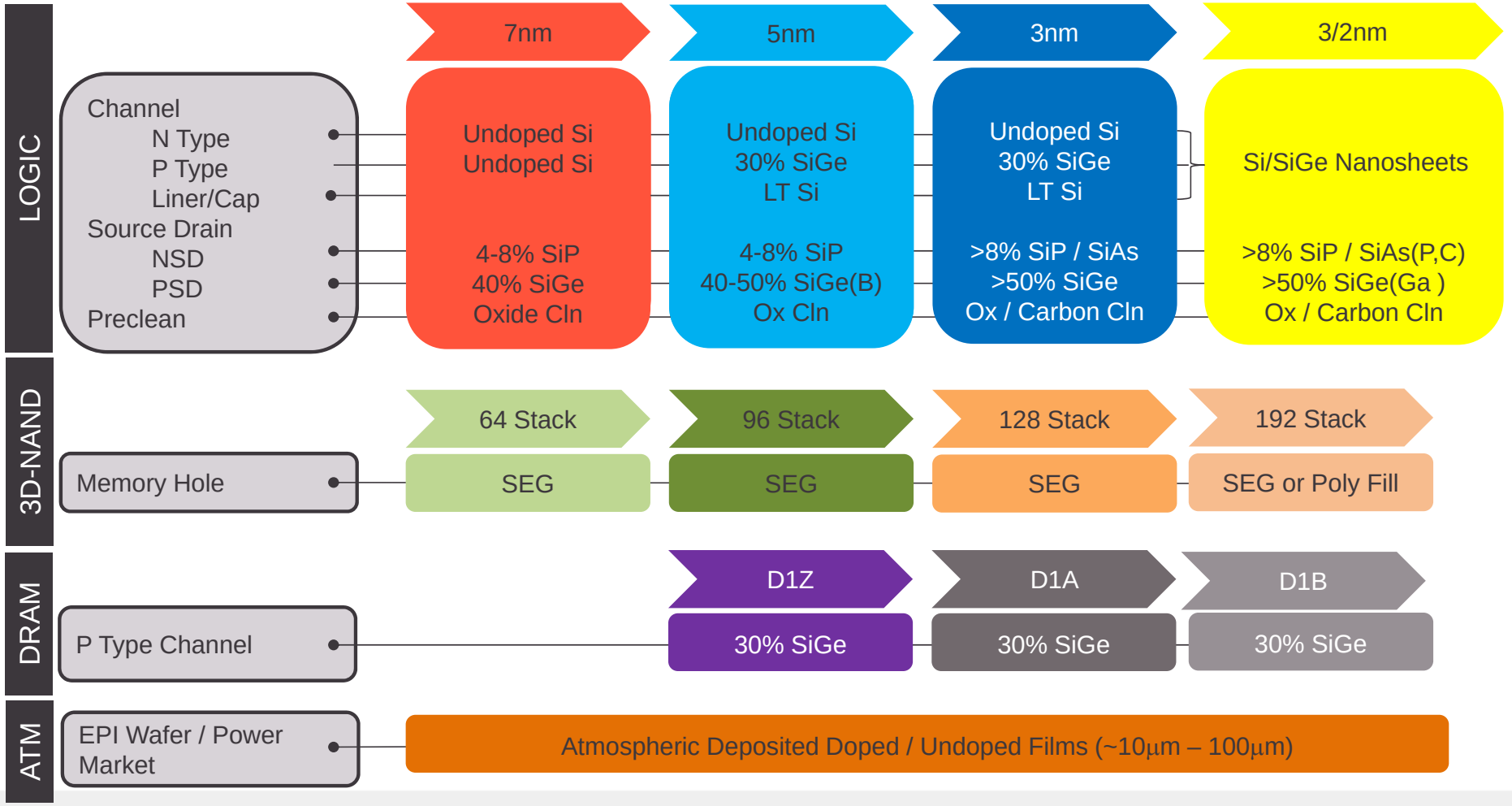
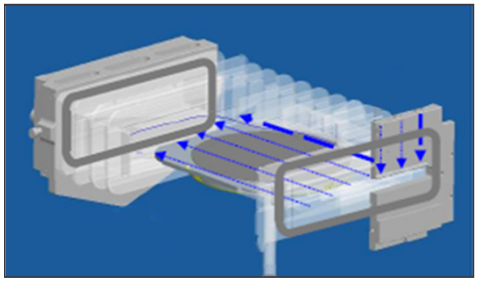
EPI CRITICAL PROCESS APPLICATIONS



INTREPID® ES KEY DESIGN FEATURES

Intrepid® ES

Low Volume Chamber with Laminar Flow

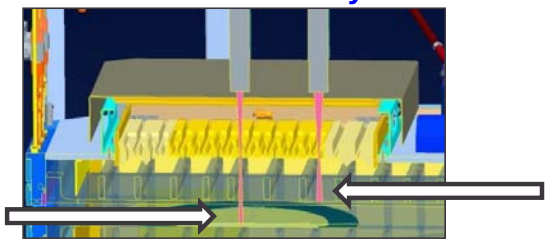


→ Superior uniformity with low CoO

AEGIS/10-PORT Gas Injection

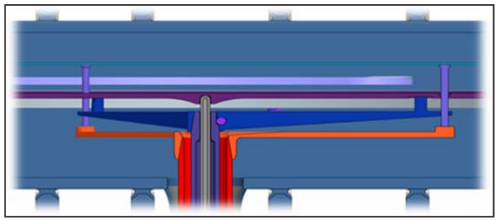
→ Real-time read back and active flow control

Isothermal Chamber with Pyro Addition



→ 1 Quartz temp Pyro for Isothermal Chamber control: TTTM, MWBC
→ 1 Wafer Pyro for Wafer Temp Control, SPC and diagnostics

Low Mass Susceptor

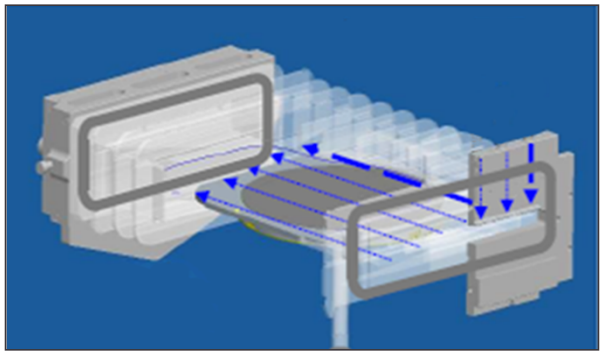


→ Higher Tput w/ Fast ramp up and ramp down temp transitions

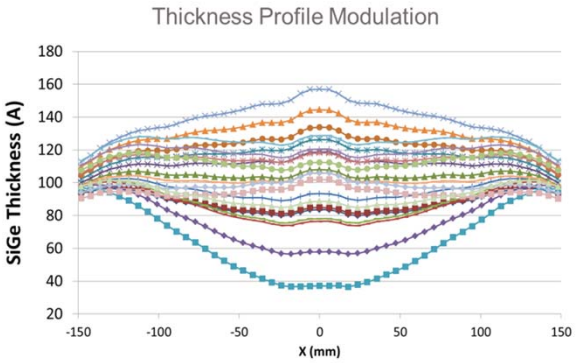
Intrepid ES delivers *isothermal* process modules for improved film performance with high throughput

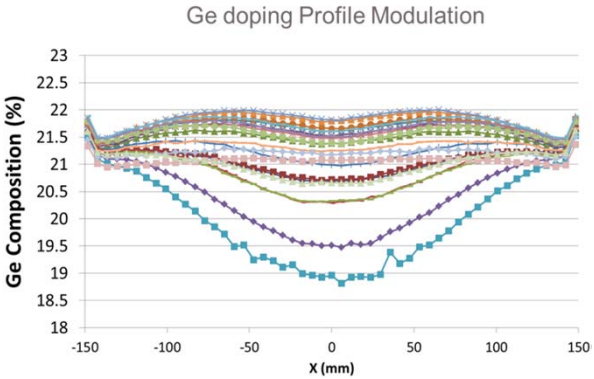
INTREPID® ES:
SUPERIOR DOPANT AND THICKNESS PROFILE TUNABILITY

Low Volume Chamber with Laminar Flow

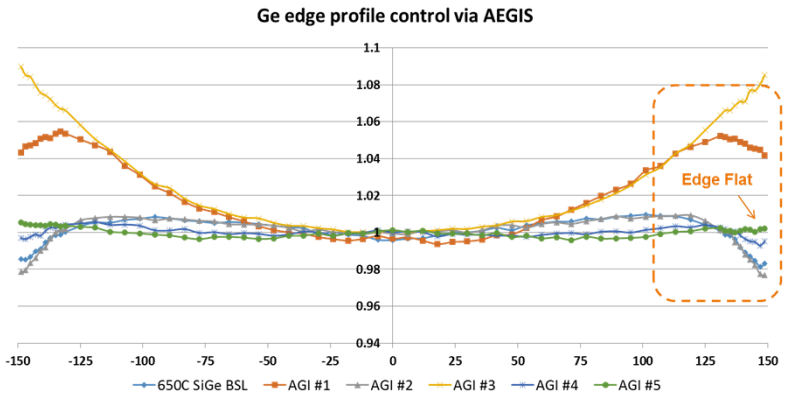


AEGIS/10-PORT Gas Injection





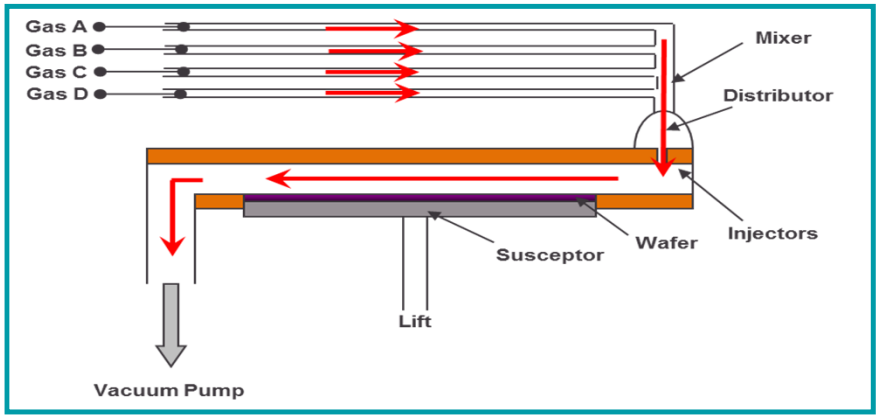
Laminar Flow combines with AEGIS to generate various thickness and Ge% tunability



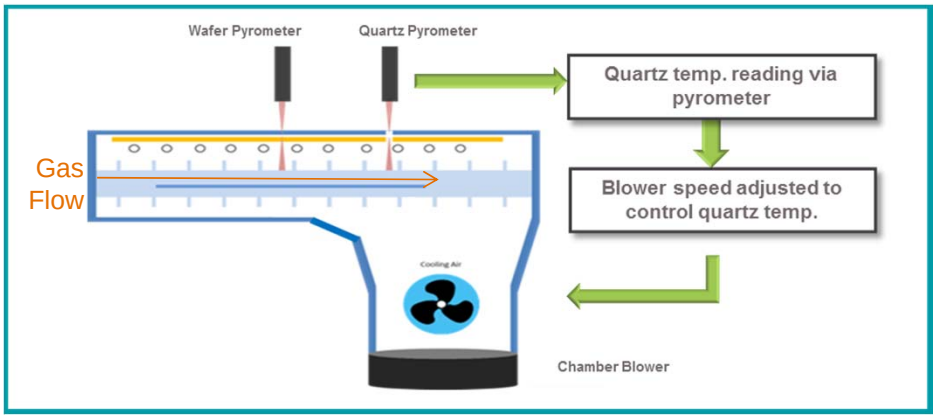
AEGIS Allows for Ge% Profile Tuning at the far wafer edge (1.2mm)

INTREPID® ES: ISOTHERMAL CHAMBER ADVANTAGE

PULSAR: CROSS-FLOW, HOT WALL REACTOR



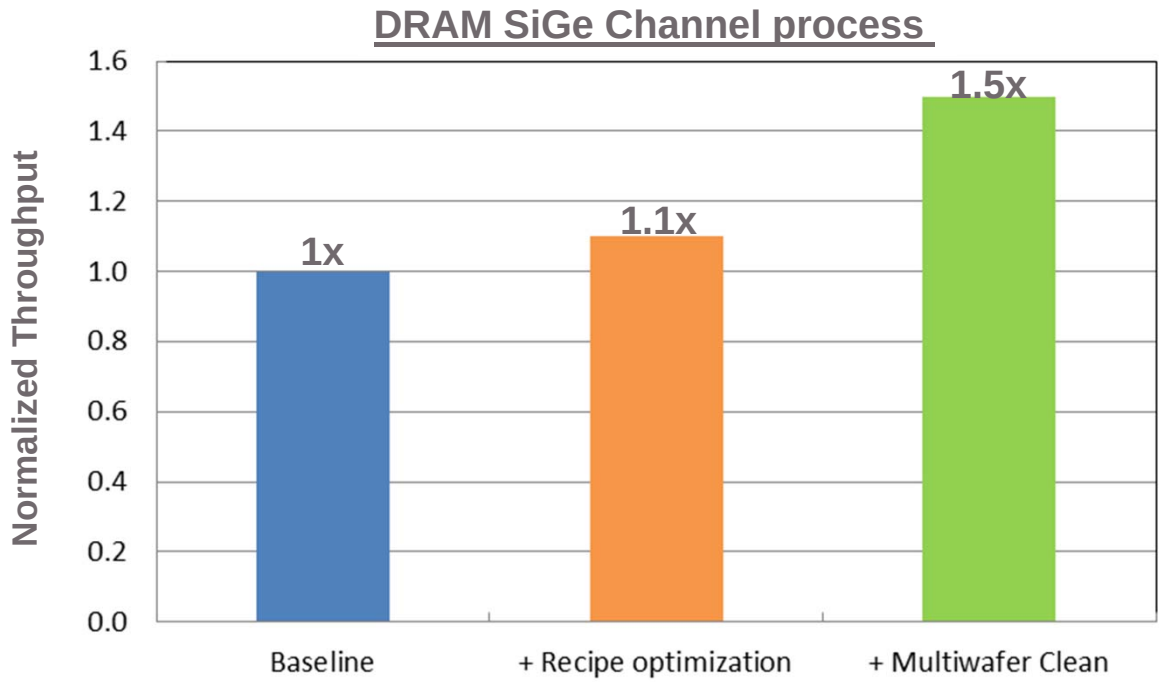
INTREPID ES: CROSS-FLOW, ISOTHERMAL REACTOR



Application	Quartz Temp, Clean	Quartz Temp, Deposition	MWBC
Si Channel, DCS, 1500A	680	550	>30k
Si Channel SiH4, 500A	650	300	>25k
SiGe Channel, SiH4/GeH4, 500A	650	350	>25k
LT Si capping/liner, 20A	600	250	Under evaluation
SiP with P up to 8at. %, SiAs, SiAsP	680	350	>15k
SiGeB	680	350	Under evaluation

Controlling quartz temperature during deposition and chamber cleans has proven to show excellent WTW performance and long MWBC cycles

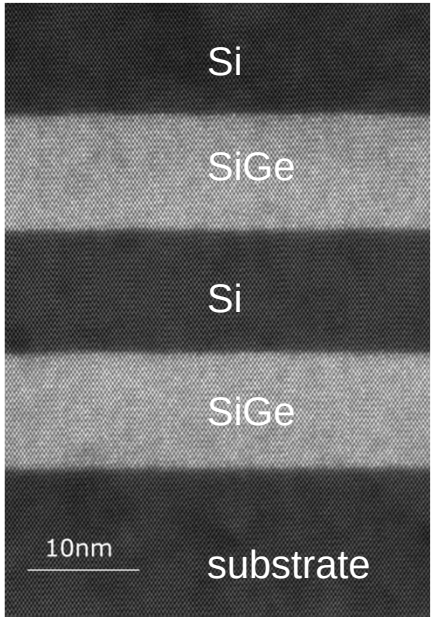
INTREPID® ES:
ISOTHERMAL CHAMBER ENABLES HIGH PRODUCTIVITY



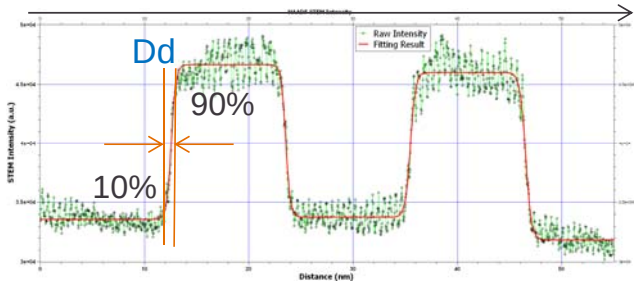
50% Throughput increase from starting recipe compared to new optimized 25x multi-wafer clean recipe

ASM NANOSHEET DEVELOPMENT: INTERFACE TRANSITION THICKNESS MINIMIZATION

Key Requirement: Transition width between the Si and SiGe layers needs to be minimized to <5A. This width directly influences the shape of the wire/sheet after etch.



Intensity profile*



Interface #	Average Dd (Å)
1 (Si substrate ->SiGe)	4.9
2 SiGe->Si	3.7
3 Si->SiGe	3.8
4 SiGe->Si	5.4

~5A interface transition thickness *

* By TEM Z-contrast line scan analysis

ASM isothermal chamber design + AEGIS flow control will enable customers to move forward with nanosheet development

ASM EPI ADVANTAGES

- **Film tunability: low chamber volume with AEGIS = best in class thickness and dopant profile tuning**
- **Isothermal hot wall chamber: long MWBC cycles, cleaner chamber for defectivity, and multi-wafer clean for high throughput**
- **Significant push for reducing EPI costs for our customers. Continuous focus on throughput improvement, wafer edge yield, and PM extension**
- **ASM hardware solutions enable current and future customer film needs**

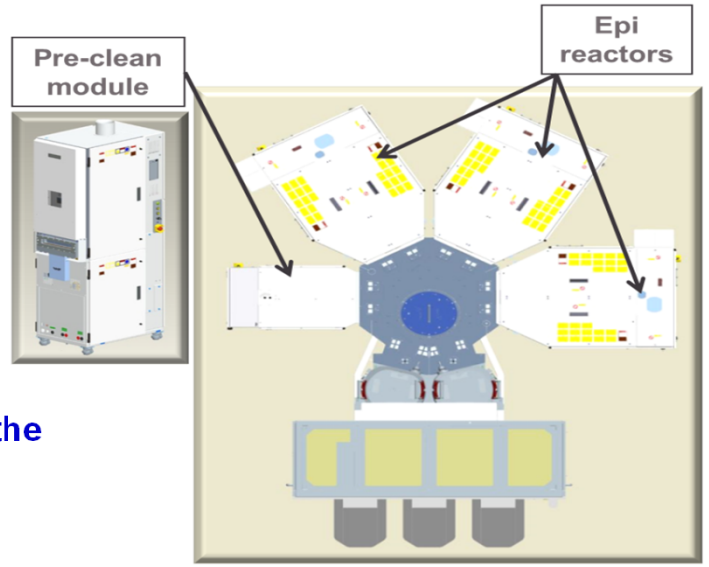
OUTLINE

- **Device and Technology trends driving the ALD market**
  - Logic
  - Memory
  - Patterning
- **ALD**
  - ASM ALD Products
  - Selected applications in Logic, 3D-NAND, DRAM and Emerging Memory
- **PECVD**
- **Vertical Furnace**
- **Epitaxy**
  - Epi process applications
  - Intrepid ES features and benefits
- **Epitaxy – Introducing Previum®**
  - Previum® features & benefits

PREVIUM INTEGRATED PRE-CLEAN INTRODUCTION

What is Previum?

- It is an integrated EPI preclean offering from ASM
  - It removes 15-20 monolayers of native oxide from the initial substrate before EPI deposition.



Why is Previum Needed?

- Surface cleaning (removal of carbon and native oxide) is critical to enable high quality EPI film growth. **All Advanced Logic devices run in the world today utilize an integrated preclean for highest quality EPI growth**

How does Previum Process Work?

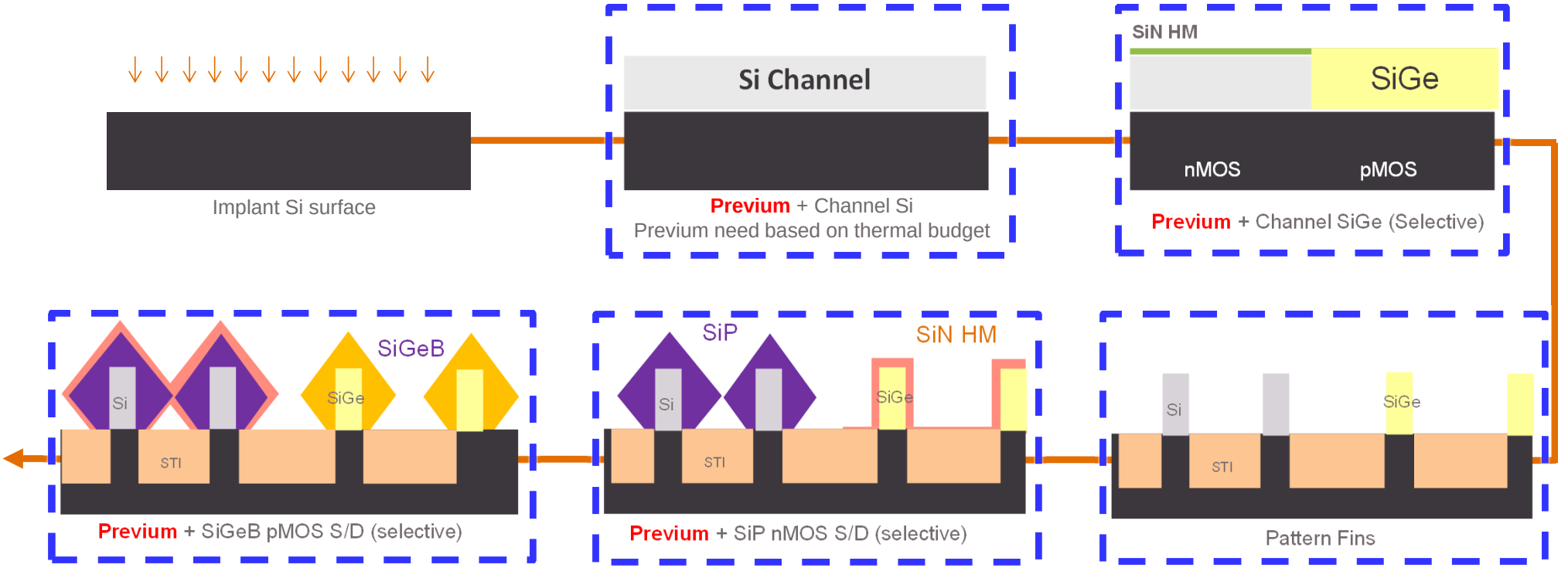
- It is based on a chemical etch process (no direct plasma)

Gas → RPU → Reactive Species → Chamber

1) Surface Chemical Conversion
2) Sublimation of converted layer

Previum is an integrated Preclean Chamber to enable high quality EPI Film Growth

PREVIUM® PRE-CLEAN IN LOGIC PROCESS FLOW

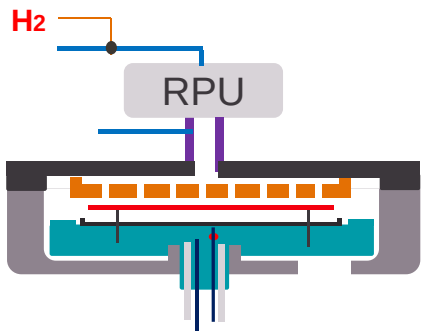


Simplified Logic Process Flow Highlights the Need for Multiple Integrated Previum Surface Cleaning Steps

PREVIUM® PRE-CLEAN PROCESS FLOW

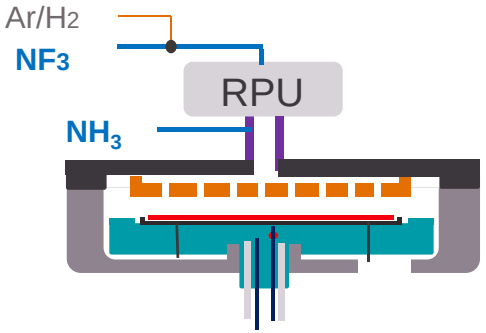
Previum Surface Cleaning Consists of 3 Process Recipe Steps for Carbon and Oxide Removal

Carbon removal with H_2 through RPU



$C+H^* \rightarrow C_xH_y$ (g)

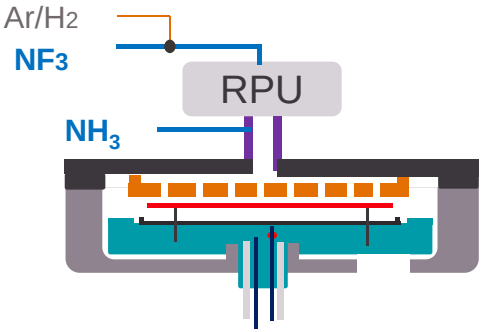
Oxide conversion with wafer on cold susceptor



$NH_4F_{(g)} + SiGeO_{2\,(s)} \rightarrow (NH_4)_2SiF_{6\,(s)} + (NH_4)_2GeF_{6\,(s)} + H_2O_{(g)} + ...$

Wafer temperature 50 °C

Salt sublimation with wafer held close to hot showerhead



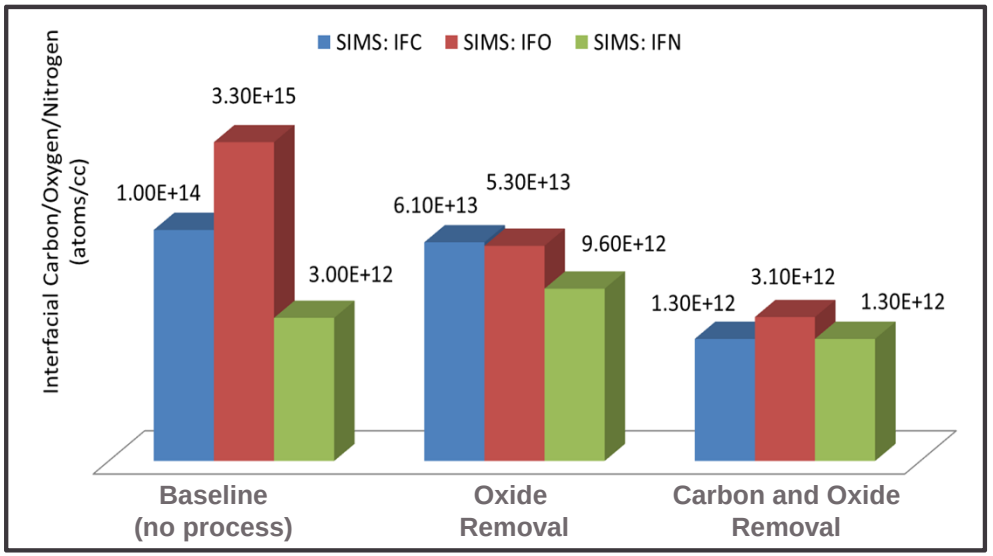
$(NH_4)_2SiF_{6\,(s)} + (NH_4)_2GeF_{6\,(s)} \rightarrow NH_3\,(g) + SiF_4(g) + GeF_4\,(g) + ...$

Wafer temperature <225 °C

Previum Process Optimized for Wafer Surface Cleaning at Low Temperatures

PREVIUM® PERFORMANCE: EFFECTIVENESS OF SURFACE CLEANING PROCESS

- **Primary purpose of the Previum process is to remove wafer surface contamination:**
  - → Oxygen in the form of SiO_2 (either native oxide or from previous processing steps)
  - → Carbon and Nitrogen (from atmospheric contamination and/or previous processing steps)



~100x reduction in O (compared to baseline)

~100x reduction in C
~1000x reduction in O (compared to baseline)

Previum Surface Clean Shows Significant Contamination (Carbon and Oxygen) Reduction

PREVIUM® PERFORMANCE: OXIDE/NITRIDE SELECTIVITY

- **Device pattern wafers can have several different materials on the surface. The preclean process needs to remove oxide and carbon highly selective towards these materials.**
  - → Typical metric compares removal of oxide compared to nitride with a target of >10 Ox/Nit Selectivity

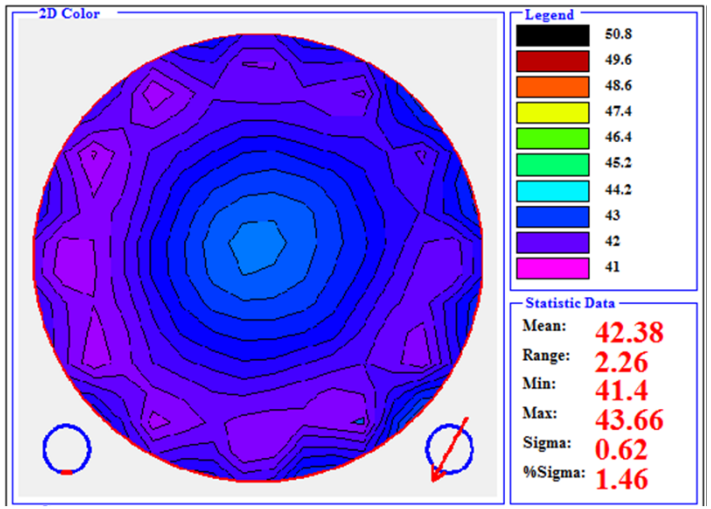
	Removal target Nitride wafer type	Oxide Removal (Å)	Nitride Removal (Å)	Selectivity
Previum	40A of Oxide removal Compared to PEALD nitride	43.5	0.38	**114.4**

Previum Process Easily Exceeds Oxide/Nitride Selectivity Target

PREVIUM® PERFORMANCE: OXIDE REMOVAL UNIFORMITY

Oxide removal uniformity across the wafer is extremely important to achieve consistent, uniform EPI growth and uniform device performance

- Tight tolerance in within wafer removal uniformity is achieved through optimized chamber hardware:
  - → Etchant gas is evenly distributed across a specialized showerhead configuration
  - → Temperature is maintained within a range of < 1ºC across the wafer using active heating and cooling components in the susceptor



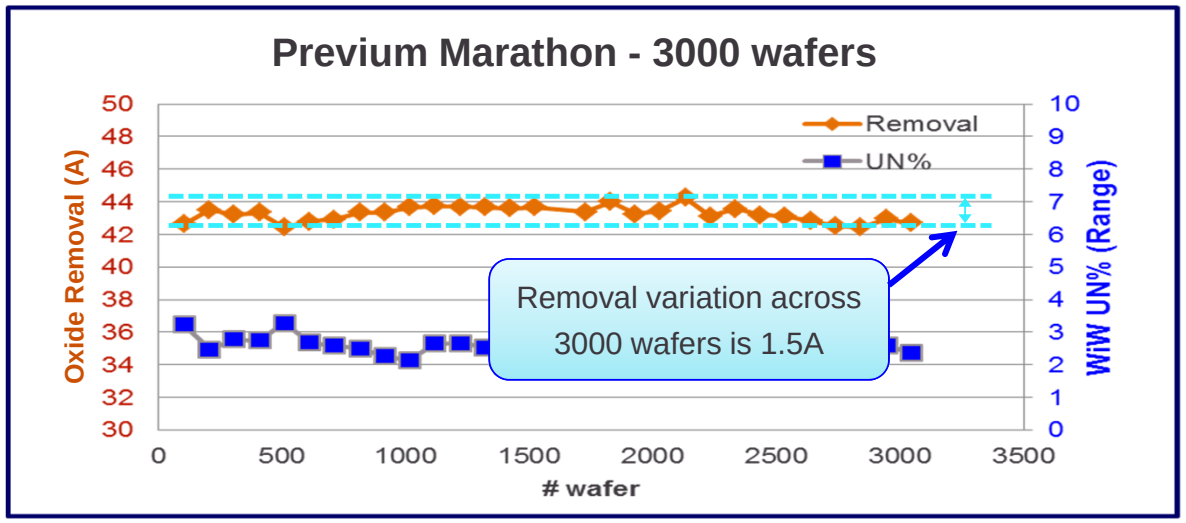
Oxide removal range across a 300 mm is typically <2.5A

Si **Atomic diameter of a Si atom is 2.6 A**

Previum Uniformly Removes Oxide Across the Wafer Surface

PREVIUM® PERFORMANCE: PROCESS REPEATABILITY

Oxide Removal



Average Oxide Removal (Å)	43.3
Wafer to Wafer Removal Uniformity	1.1%

Particle Performance

Monitor Wafer No.	Adders
258	0
512	0
765	2
1018	0
1272	1
1526	2
1779	3
2033	0
2286	4
2539	4
2792	8
3046	1

Average adders: 2.1, >32nm

Repeatable Oxide Removal Demonstrated with Low Defectivity

PREVIUM® INTEGRATED PRE-CLEAN SUMMARY

- **Previum Integrated Surface Cleaning needed for high quality EPI film growth**
  - → Carbon and Oxide removal in the same process recipe in the same process chamber
- **Enables multiple EPI steps in advanced Logic Devices**
- **Process and hardware optimized to achieve required performance**
  - → Interface contamination removal
  - → Oxide removal selectivity to Nitride
  - → Within wafer removal uniformity
  - → Wafer to wafer and defect performance

THANK YOU